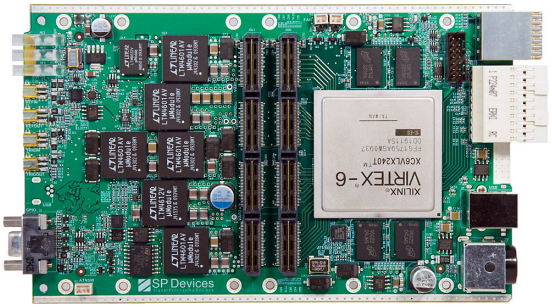
ADQDSP Datasheet

ADQDSP is a digital signal processing board for signal recording and real-time signal processing. Powered with a Virtex 6 LX240T FPGA and 1GByte data RAM and peer-to-peer streaming, it operates as a calculation enhancement to the ADQ V6 Digitizer family. The ADQDSP also operates as a stand alone calculation board.



Introduction

The ADQDSP is a digital signal processing board, tailored for real-time signal processing. The ADQDSP connects through peer-to-peer streaming to any ADQ V6 digitizer. It is possible to place a chain of ADQDSP units for extreme calculation tasks.

The FPGA is a Virtex 6 LX240T. The FPGA firmware consist of supporting functions, for example PCIe controller and DRAM controller. Parts of the FPGA are available for customized real-time applications through the ADQDSP Development Kit.

The ADQDSP provides host connection through various interfaces and form factors.

ADQDSP Development Kit

SP Devices' ADQDSP Development Kit is an required tool for integrating custom real-time signal processing in the FPGA. The custom firmware is easily integrated into the digitizer's standard functions to enhance the capabilities of demanding signal analysis. More details about this product can be found in the datasheet for the ADQDSP Development Kit.

Ordering information

ORDERING INFORMATION	
Order code	ADQDSP
AVAILABLE OPTIONS	
cPCIe / PXIe interface	–PXIE
PCIe interface	–PCIE
Micro-TCA interface	–MTCA
RELATED PRODUCTS	
ADQDSP Development Kit	

Features

- Virtex 6 FPGA
- Peer-to-peer data streaming mode
- 1 GByte data memory
- Trigger in
- Trigger out
- Clock reference in
- Clock reference out
- GPIO
- Data interfaces cPCIe / PXIe / PCIe / MTCA.4
- 3.2 GBytes/s data transfer rate on Gen2 by 8 lanes
- Open FPGA for real-time custom applications

Applications

- Time-of-flight
- Physics experiments
- LIDAR
- Wireless communication
- Optical transmission
- High-speed data recording
- Test and measurement
- Ultrasonic ranging

1 Technical data[1]

Table 1:

KEY PARAMETERS	
Data memory	8 Gbit
Memory bandwidth	96 Gbit/s
Host computer interface	3.2 GByte/s sustained data rate over 8 lanes PCIe Gen2
Trigger	Software / External
Number of GPIOs	5
Clock reference	Internal / External

Table 2:

CLOCK REFERENCE INPUT		
Internal clock reference		
Frequency	10	MHz
Accuracy	± 5 ± 0.5/y	ppm
External clock reference		
Frequency (min – max)	1 – 250	MHz
Signal level (min – max)	0.8 – 3.3	V_{PP}
Impedance AC	50	Ω
Duty cycle	50% ± 5%	
Connector PCIe / PXIe	MCX	
Connector MTCA.4	MMCX	
PXIe clock reference[1]		
PXIe clock	100	MHz
PXIe sync[2]	10	MHz

1. Available on PXIe form factor only.
2. Jitter reduced by PXIe clock in digitizer.

Table 3:

CLOCK REFERENCE OUTPUT		
Frequency	Same as clock reference	
Signal level	3.3	V_{PP}
Impedance AC	50	Ω
Duty cycle	50% ± 5%	
Connector PCIe / PXIe	MCX	
Connector MTCA.4	MMCX	

Table 4:

EXTERNAL TRIGGER INPUT		
Input impedance DC	50	Ω
Input range (min – max)	–0.4 to 2.4	V
Threshold rising/falling edge	500	mV
Sensitivity	200	mV
Jitter	25	ps
Resolution	1/FS	s
Connector PCIe / PXIe	MCX	
Connector MTCA.4	MMCX	

Table 5:

TRIGGER OUTPUTS		
Output impedance	30	Ω
Output (low – high)	0.1 – 3.2	V
Connector PCIe / PXIe	MCX	
Connector MTCA.4	MMCX	

Table 6:

GPIO		
Number of GPIO	5	
Output impedance pin #5	33	Ω
Output impedance pin #1–4	100	Ω
Output (low – high)[1]	0.1 – 3.2	V
Input impedance	10	kΩ
Input (low – high)	1 – 2.3	V
Connector	Micro-D plug 9 way	

1. Unloaded condition.

Table 7:

POWER SUPPLY		
Supply Voltage	12	V
Power[1]	30	W
Connector PCIe	6-pin ATX power	
Connector cPCIe/PXIe	from slot	
Connector MTCA	from slot	

1. This is an estimated value from typical use case. The power consumption is set by the custom firmware.

Table 8:

CERTIFICATION AND COMPLIANCE
CE

Table 9:

LED INDICATORS		
Power	Green	Power up
Ready	Yellow	User control
Status	Red	Flashing overheat

1. All values are typical unless otherwise noted.

2 Architecture

2.1 Block diagram

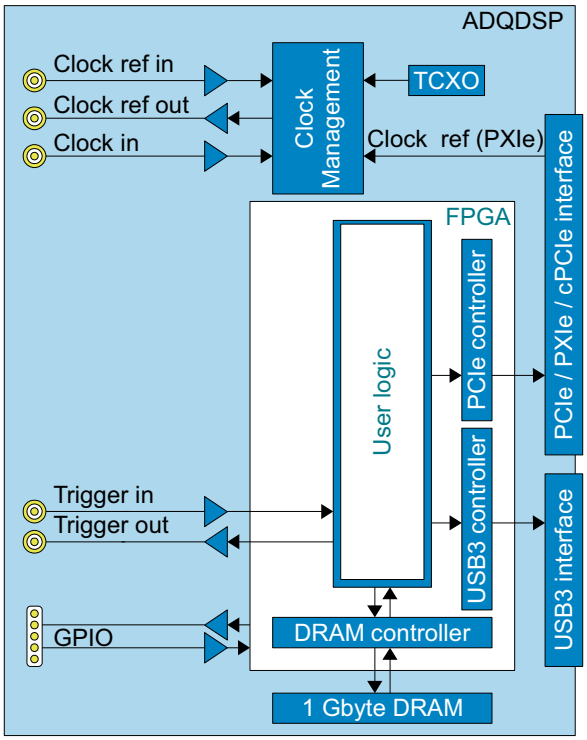


Figure 1: Block diagram.

A block diagram of the ADQDSP is shown in **Figure 1**. The main blocks are described below. The ADQDSP contains a framework for signal processing. All signal processing has to be designed using the ADQDSP Development Kit.

3 Functional overview

3.1 Data streaming

Data is streamed to the ADQDSP via the PCIe interface. After processing, data is streamed out via the PCIe interface.

To support data recording, there is on-board DRAM of 1 GBytes.

3.2 Signal processing

Custom real-time signal processing can be implemented using the ADQDSP Development Kit.

3.3 Trigger

There is support for are several trigger modes;

- External trigger for synchronization
- Software trigger for user's control

There is also a trigger output for triggering external equipment.

3.4 Clock

There are several modes for clocking the ADQDSP;

- Internal 125 MHz clocks for PCIe interface
- Internal 200 MHz clock for DRAM internface
- Internal 75 MHz general purpose clock
- External clock reference for synchronization

There is also a clock reference output for clocking external equipment.

3.5 GPIO

There are 5 GPIO pins for real-time communication with external equipment. The GPIOs are controlled from software, but can also be accessed from the ADQDSP Development Kit for integration in a real-time control system.

The connector is Micro DSUB 9 way plug. A suitable socket with lead is for example MOLEX 83421-9044.

#	Function
1	GPIO pin #1
2	GPIO pin #2
3	GPIO pin #3
4	GPIO pin #4
5	GPIO pin #5
6	GND
7	GND
8	GND
9	GND

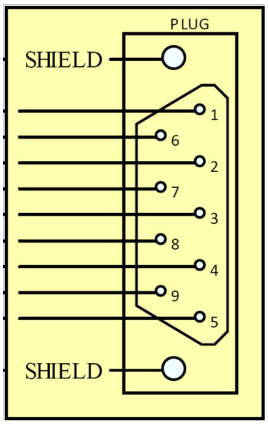


Figure 2: GPIO connector.

4 Absolute maximum ratings

Exposure to conditions exceeding these ratings may reduce lifetime or permanently damage the device.

The ADQDSP has a built-in fan to cool the device. The built-in temperature surveillance unit will protect the ADQDSP from overheating by temporarily shutting down parts of the device in such a situation.

Table 10:

ABSOLUTE MAXIMUM RATINGS	MIN	MAX
Supply voltage (to GND)	–0.4 V	14 V
Trigger input (to GND)	–3 V	3.7 V
Clock ref (AC)		3.3 V_{PP}
GPIO input (to GND)[1]	–1 V	4.6 V
Ambient temperature (operation)	0 °C	45 °C

1. A voltage on a GPIO input higher than 3.3 V may change the output voltage on GPIOs which are set to outputs. This may damage external equipment.

5 Software tools

5.1 Operating systems

The software package includes drivers for the main operating systems.

Table 11:

OPERATING SYSTEM	
Windows 7	32 bit and 64 bit
Windows 8	32 bit and 64 bit
Windows 10	When available
Linux[1]	Kernel 2 and 3, 32 and 64 bits

1. Contact SP Devices sales representative for information about distributions.

5.2 Software development kit (SDK)

The ADQDSP digitizer is easily integrated into the application by using the software development kit. The SDK is included with the ADQDSP.

The SDK is the tool for integration the software part of the design that execute on the host PC. The SDK is also used for setting up data streaming to and from the ADQDSP.

The firmware in the ADQDSP FPGA is designed using ADQDSP Development Kit, which is purchased separately.

6 Data interface options

The ADQDSP is available in several form factors to suit various integration situations. The form factor sets the communication interface to the host PC as well as the mechanical properties of the ADQDSP.

The cPCIe, PXIe and M-TCA.4 from factors are intended for integration into a rack for modular instrumentation or large scale acquisition.

The PCIe form factor is for integration into the host PC. The board is half length to enable compact solutions.

Also the PCI-Express based models are equipped with a USB2.0 interface. It is intended for restoring the system if a custom firmware upload has failed.

6.1 PCI Express interface

The PCI Express interface is intended for integration in a PC.

Table 12:

PCIe INTERFACE		
Data rate	Gen2	
Bus width electrical	8	lanes
Sustained data rate, 8 lanes[1]	3.2	GByte/s
Bus width mechanical[2]	16	lanes
Board height	2	slots
Board length (half length)	167	mm

1. This is depending on the capacity of the complete system including the selected PC.
2. The wide contact is required to support the weight of the board.

Order code: –PCIE

6.2 cPCIe / PXIe interface

The ADQDSP is available with cPCIe / PXIe interface.

Table 13:

cPCIe / PXIe INTERFACE		
Bus width	8	lanes
Bus peak capacity	16	Gbit/s
Sustained data rate[1]	3.2	GByte/s
PXIe card size	3U 2 slot 8TE	

1. This is depending on the capacity of the complete system including the selected PC.

Order code: –PXIE

6.3 Micro-TCA interface

The ADQDSP is available with digital back-end and interfaces for Micro-TCA chassis, **Figure 3**.

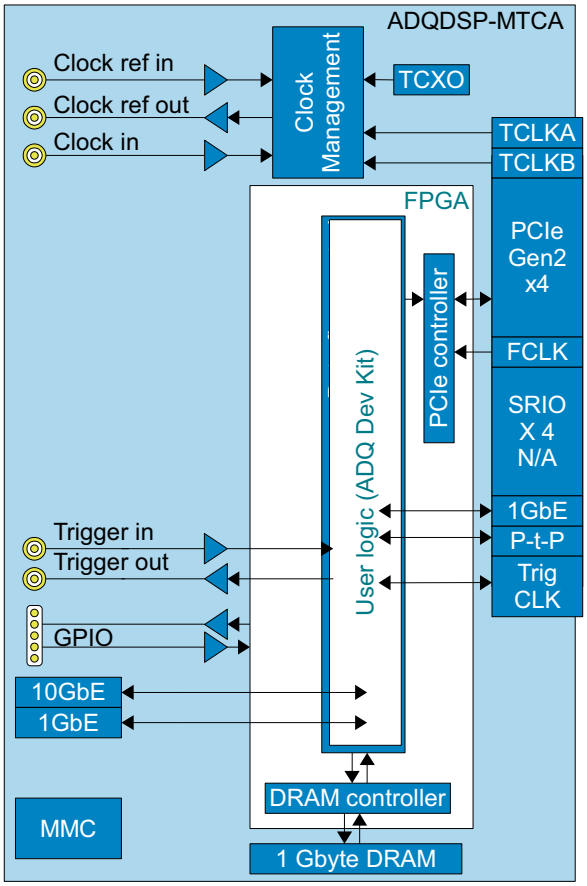


Figure 3: Block diagram of ADQ1600-MTCA.

Table 14:

MICRO-TCA BOARD SIZE	
Board width	Double width
Board height	Mid-size

Some of the pins in the backplane connector are used for the standard digitizer functions. Some are available for custom design using the ADQDSP Development Kit for custom implementations only.

Table 15:

MICRO-TCA INTERFACE		
Signal	**Port**	**Status**
1GbE	0	ADQDSP Dev Kit
PCIe	4-7	Standard
Point-to-point	12-15	ADQDSP Dev Kit
Trigger, Data, Clocks	17-20	ADQDSP Dev Kit
TCLKA	Clk 1	Standard
TCLKB	Clk 2	Standard
FCLKA	Clk 3	Standard

Table 16:

FRONT PANEL ADDITIONAL INTERFACE		
Signal	**Connector[1]**	**Status**
1 GbE	SFP	ADQDSP Dev Kit
10 GbE	SFP+	ADQDSP Dev Kit

1. **SFP+ and SFP modules are not included.**

Figure 4: Typical Micro-TCA card

Order code: –MTCA

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