

## ADQ32-PDRX Datasheet



The ADQ32-PDRX is a high-speed digitizer with extended dynamic range for pulse data applications. The ADQ32-PDRX features:

- One analog input channel
- 12 bits resolution
- 3 bits dynamic range extension through built-in dual-gain channel combination
- 2.5 GSPS sampling rate
- 7 GByte/s sustained data transfer rate
- Two external triggers
- General Purpose Input/Output (GPIO)
- Open FPGA for real-time signal processing
- Firmware option for averaging of records

### Ordering information

- ADQ32-PDRX digitizer including firmware FWDAQ, order code [ADQ32-PDRX](#). FWDAQ includes license key “FWPDRX” for activating channel combination functions.
- ADQ32 digitizer with warranty extension to 5 years, order code [ADQ32-W5Y](#).<sup>1</sup>
- Firmware development kit for FWDAQ, order code [ADQ32-DEVDAQ](#).
- Firmware option averaging, order code [ADQ32-FWATD](#).

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<sup>1</sup> Included warranty is 3 years from the date the product is shipped by Teledyne SP Devices. The option extends the warranty to 5 years from the date the product is shipped by Teledyne SP Devices. Warranty extension must be ordered before included 3 years warranty is expired.

## 1 ADQ32-PDRX INTRODUCTION

### 1.1 Features

- One input channel
- 2.5 GSPS sampling rate
- 12 bits resolution
- 3 bits dynamic range extension through built-in dual gain channel combination
- DC-coupled with 760 MHz bandwidth
- Programmable DC offset
- Internal and external clock reference
- Internal and external sampling clock
- Clock reference output
- Internal and external triggers
- 8 GBytes data memory
- 7 GByte/s sustained data streaming to CPU and GPU
- Data interface PCIe Gen3 x8
- Averaging firmware FWATD

### 1.2 Applications

- Time-of-flight mass spectrometry
- LIDAR
- Pulse data systems

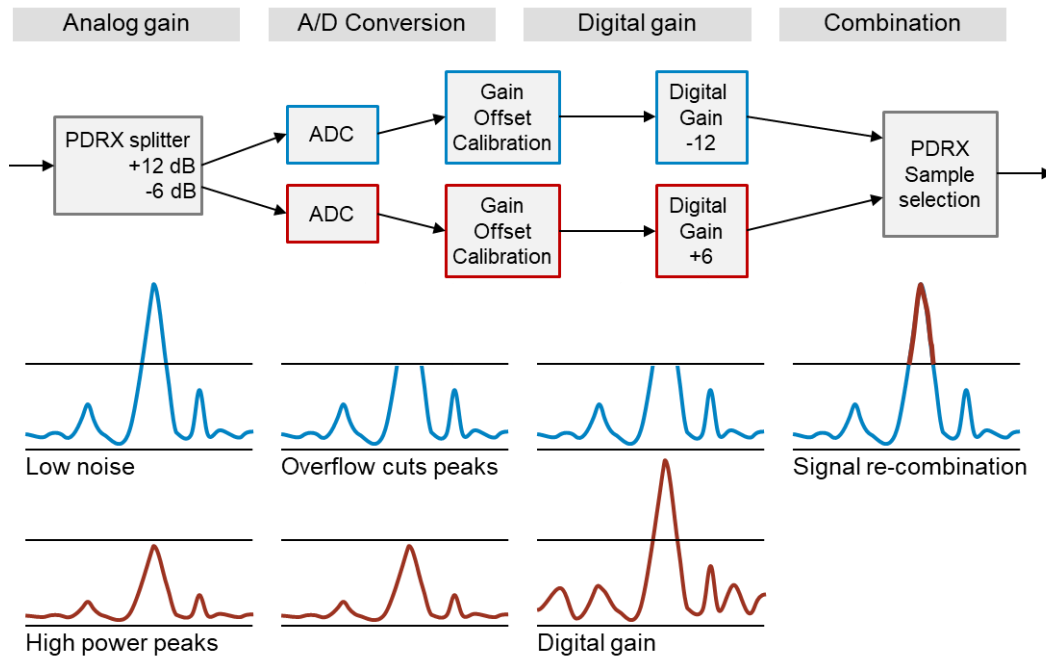
### 1.3 Advantages

- ADQ32-PDRX integrates the analog dual-gain amplifier for a compact high-performance system solution
- Real-time processing for pulse data capture and high data throughput
- Teledyne SP Devices' design services are available for fast integration to reduce time-to-market

### 1.4 System design optimization; open FPGA and streaming to CPU and GPU

High-performance data acquisition systems require high speed real-time analysis. ADQ32-PDRX uses a built-in dual-gain channel combination to increase the dynamic range in pulse capture. Weak pulses are captured through a channel with high gain and strong pulses are captured through a channel with low gain. The channel combination results in a dynamic range extension equivalent to 3 extra bits of vertical resolution.

The PDRX channel combination is carried out by the digitizer firmware and is available for [FWATD](#) and [FWDAQ](#).



**Figure 1 Principle of channel combination**

To make the most of the increased dynamic range, secondary effects on the signal quality must be dealt with. Impedance matching is managed by an equalizer and reflection cancellation. Baseline fluctuations are managed by filtering.

In addition to the specific pulse detection, ADQ32-PDRX supports a variety of options for efficient system design:

#### Streaming to GPU

ADQ32-PDRX supports up to 7 GByte/s peer-to-peer streaming and streaming via pinned buffer to GPU. A GPU offers a powerful platform for implementing application-specific signal processing algorithms.

#### Streaming to CPU

ADQ32-PDRX supports up to 7 GByte/s to host computer. Implementing the application-specific algorithms in the CPU results in an efficient system.

#### Open FPGA for real-time processing

ADQ32-PDRX offers an open FPGA for implementation of the application-specific computations in the FPGA. This gives the most compact system design. Firmware development kit is ordered separately.

## 2 TECHNICAL DATA

Technical parameters are valid for ADQ32-PDRX operating with firmware FWDAQ. All parameters are typical unless otherwise noted.

**Table 1 Analog input (front panel label A)**

Parameter	Condition	Min	Typical	Max	Unit
<b>Basic parameters</b>					
Number of channels			1		
Sampling rate			2.5		Gsample/s
Bandwidth	-3dB		730		MHz
Input range			1		Vpp
Input impedance			50		Ω
Coupling			DC		
Connector type			SMA		
<b>Programmable DC-offset</b>					
DC-offset range		-0.5		+0.5	V
<b>Dynamic performance</b>					
Idle channel noise <sup>2</sup>			71		dBFS
ENOB noise based <sup>3</sup>			11.6		bits

**Table 2 Comparison of ADQ32-PDRX to ADQ32**

Parameter	Condition	ADQ32	ADQ32-PDRX	Unit
RMS noise	Terminated input	244	96	μV
Max input range		0.5	1	Vpp
DC-offset		-0.25 to 0.25	-0.5 to 0.5	V
Dynamic range <sup>4</sup>		57.2	71.3	dB
ENOB <sup>5</sup>		9.2	11.6	bits
DC-offset		-0.25 to 0.25	-0.5 to 0.5	V
Bandwidth	-3dBFS	1000	760	MHz
Attenuation at 1GHz		3	5.1	dB

<sup>2</sup> Measured integrated noise with a terminated input. Noise level is computed relative a full-scale sine wave.

<sup>3</sup> Computed from idle channel noise. See figure for ENOB at sweep of input power.

<sup>4</sup> Power of full-scale sine wave relative noise with terminated input.

<sup>5</sup> Computed from “Dynamic Range” in Table 2 using the formula (Dynamic Range – 1.76) / 6.02.

**Table 3 Clock generator and front panel CLK connector.**

Parameter	Condition	Min	Typical	Max	Unit
<b>Internal clock reference</b>					
Frequency			10		MHz
Accuracy			±3 ±1/year		ppm
<b>Internal sampling clock generator <sup>6</sup></b>					
Frequency range 1		2440	2500	2500 <sup>7</sup>	MHz
Frequency range 2		1840		1970	MHz
<b>External clock reference input (from front panel CLK connector)<sup>8</sup></b>					
Frequency		1	10	500	MHz
Frequency <sup>9</sup>	Jitter cleaner enabled	10 -10 ppm	10	500 +10 ppm	MHz
Frequency	Delay line used		10	100	MHz
Delay line tuning range <sup>10</sup>			500		ps
Signal level		0.5		3.3	Vpp
Input impedance	AC		50		Ω
Input impedance	DC		10k		Ω
Input impedance (high) <sup>11</sup>	AC		200		Ω
<b>Clock reference output (on front panel CLK connector)<sup>12</sup></b>					
Frequency			10		MHz
Signal level	Into 50-Ω load		1.2		Vpp
Output impedance	AC		50		Ω
Output impedance	DC		10k		Ω
<b>External direct sampling clock input (from front panel CLK connector)<sup>13</sup></b>					
Frequency <sup>14</sup>		1000		2505	MHz
Signal level		0.5		3.3	Vpp
Impedance	AC		50		Ω
Impedance	DC		10k		Ω
<b>Physical connector label CLK</b>					
Connector type		SMA			

<sup>6</sup> The internal clock generator can generate frequencies in 2 different ranges.

<sup>7</sup> The software setting limit. The tolerance with external clock reference is up to 2505 MHz.

<sup>8</sup> Using a clock reference from an external source to synchronize the ADQ32 to the external source.

<sup>9</sup> The jitter cleaner requires the reference frequency to be a multiple of 10 MHz within ± 10ppm.

<sup>10</sup> Tuning of sampling clock phase relative to external clock reference input phase.

<sup>11</sup> Software-selectable high-impedance mode.

<sup>12</sup> The internal clock reference of the ADQ32-PDRX is made available to synchronize external equipment.

<sup>13</sup> Using an external clock while bypassing the internal clock generator.

<sup>14</sup> In single-channel mode, the sampling frequency is 2 times the external clock frequency.

**Table 4 Front panel TRIG connector**

Parameter	Condition	Min	Typical	Max	Unit
Connector type		SMA			
Used as input (or GPIO)					
Impedance	DC		50		Ω
Impedance (high) <sup>15</sup>	DC		500		Ω
Signal level	50-Ω mode	-0.5		3.3	V
Adjustable threshold	50-Ω mode	0		2.8	V
Signal level	High impedance	-0.5		5.5	V
Adjustable threshold	High impedance	0		2.3	V
Pulse repetition frequency	As trigger			10	MHz
Time resolution <sup>16</sup>	As trigger		50		ps
Update rate <sup>16</sup>	As GPIO			156.25	MHz
Used as output (or GPIO)					
Impedance	DC		50		Ω
Output level high VOH	Into 50-Ω load	1.8			V
Output level low VOL	Into 50-Ω load			0.1	V
Pulse repetition frequency				156.25	MHz

**Table 5 Front panel SYNC connector (may be used as a trigger source with reduced timing resolution)**

Parameter	Condition	Min	Typical	Max	Unit
Connector type			SMA		
<b>Used as input (or GPIO)</b>					
Impedance	DC		50		Ω
Impedance (high) <sup>15</sup>	DC		500		Ω
Signal range	50-Ω mode	-0.5		3.3	V
Adjustable threshold	50-Ω mode	0		2.8	V
Signal level	High impedance	-0.5		5.5	V
Adjustable threshold	High impedance	0		2.3	V
Pulse repetition frequency	As trigger			10	MHz
Time resolution <sup>16</sup>	As trigger		3.2		ns
Update rate <sup>16</sup>	As GPIO			156.25	MHz
<b>Used as output (or GPIO)</b>					
Impedance	DC		50		Ω
Output level high VOH	Into 50-Ω load	1.8			V
Output level low VOL	Into 50-Ω load			0.1	V
Pulse repetition frequency				156.25	MHz

<sup>15</sup> Software-selectable high-impedance mode.

<sup>16</sup> Timing properties are valid for 2.5 GSPS in 2 channel mode and 5 GSPS in 1 channel mode. Timing properties scale linearly with sampling frequency.

**Table 6 Front panel GPIO connector**

Parameter	Condition	Min	Typical	Max	Unit
<b>Connector type</b>				SMA	
<b>Used as input</b>					
<b>Impedance</b>			50		Ω
<b>Impedance (high) <sup>15</sup></b>			10		kΩ
<b>Input level high VIH</b>		2			V
<b>Input level low VIL</b>				0.8	V
<b>Update rate <sup>16</sup></b>				156.25	MHz
<b>Used as output</b>					
<b>Output Impedance</b>			50		Ω
<b>Output level high VOH</b>	Into 50-Ω load	1.5			V
<b>Output level high VOH</b>	No load	3.2			V
<b>Output level low VOL</b>	Into 50-Ω load			0.1	V
<b>Output level low VOL</b>	No load			0.1	V
<b>Update rate <sup>16</sup></b>				156.25	MHz

**Table 7 Custom GPIO expansion. See section 9.**

Parameter	Value
<b>Connector type</b>	40-pin FFC/FPC connector, pitch 0.5 mm
<b>Number of differential IO signals LVDS</b>	8
<b>Number of single-ended IO signals 3.3V</b>	5

**Table 8 Environment and mechanical parameters**

Parameter	Condition	Min	Typical	Max	Unit
<b>Power and temperature</b>					
<b>Power consumption <sup>17</sup></b>	FWDAQ		30		W
<b>Power supply</b>		10.8	12	13.2	V
<b>Operating temperature</b>	At fan inlet	0		45	°C
<b>Size</b>					
<b>Width</b>			1		slot
<b>Length</b>			225.7		mm
<b>Height</b>			111.2		mm
<b>Compliances</b>					
<b>RoHS3</b>			Yes		
<b>CE</b>			Yes		
<b>FCC</b>	Exclusion according to CFR 47, part 15, paragraph 15.103(c).				

<sup>17</sup> Power consumption depends on firmware option and use case. Power consumption is measured during acquisition and streaming of data at 5 Gbyte/s to PC.

**Table 9 Data acquisition**

Parameter	Condition	Min	Typical	Max	Unit
<b>Rearm time<sup>18</sup></b>				20	ns
<b>Acquisition memory (Data FIFO)</b>	Shared by all channels		8		Gbyte
<b>Record length</b>	2 channels mode	16		$2^{31}-1$	samples
	Combined channel	16		$2^{31}-1$	samples
<b>Pretrigger<sup>19</sup></b>		0		16 360	samples
<b>Length granularity, pretrigger</b>	2 channels mode	8			samples
	Combined channel	8			samples
<b>Trigger delay<sup>20</sup></b>		0		$2^{32}-8$	samples
<b>Length granularity, trigger delay</b>	2 channels mode	8			samples
	Combined channel	8			samples

**Table 10 Data transfer**

Parameter	Value	Unit
<b>Supported versions of data transfer standard PCIe</b>	Gen1 Gen2 Gen3	
<b>Supported number of lanes<sup>21</sup></b>	1	
	4	
	8	
<b>Data rate to CPU sustained with headers</b>	5	GByte/s
<b>Data rate to CPU sustained without headers</b>	7	GByte/s
<b>Data rate to GPU sustained without headers</b>	7	GByte/s
<b>Data rate peer-to-peer to GPU sustained without headers</b>	7	GByte/s

**Table 11 Software support**

Parameter	Value
<b>Operating system<sup>22</sup></b>	Windows Linux
<b>GUI</b>	Digitizer Studio
<b>Example code</b>	C, Python
<b>API</b>	C / C++

<sup>18</sup> Minimum time from the last sample of a record to the next trigger.

<sup>19</sup> Pre-trigger is set by assigning the parameter “horizontal offset” a negative value

<sup>20</sup> Trigger delay is set by assigning the parameter “horizontal offset” a positive value

<sup>21</sup> The ADQ30 must be installed in a 16 lanes slot or a slot with a connector with an open end.

<sup>22</sup> See 15-1494 Operating system support for a detailed listing of supported distributions.

### 3 FEATURES FOR DATA FLOW CONTROL, SYNCHRONIZATION AND PROCESSING

The ADQ32-PDRX features an advanced machine for flow control, synchronization, and signal processing. The block diagrams are shown in Figure 2 and Figure 3. The features are described in the following tables.

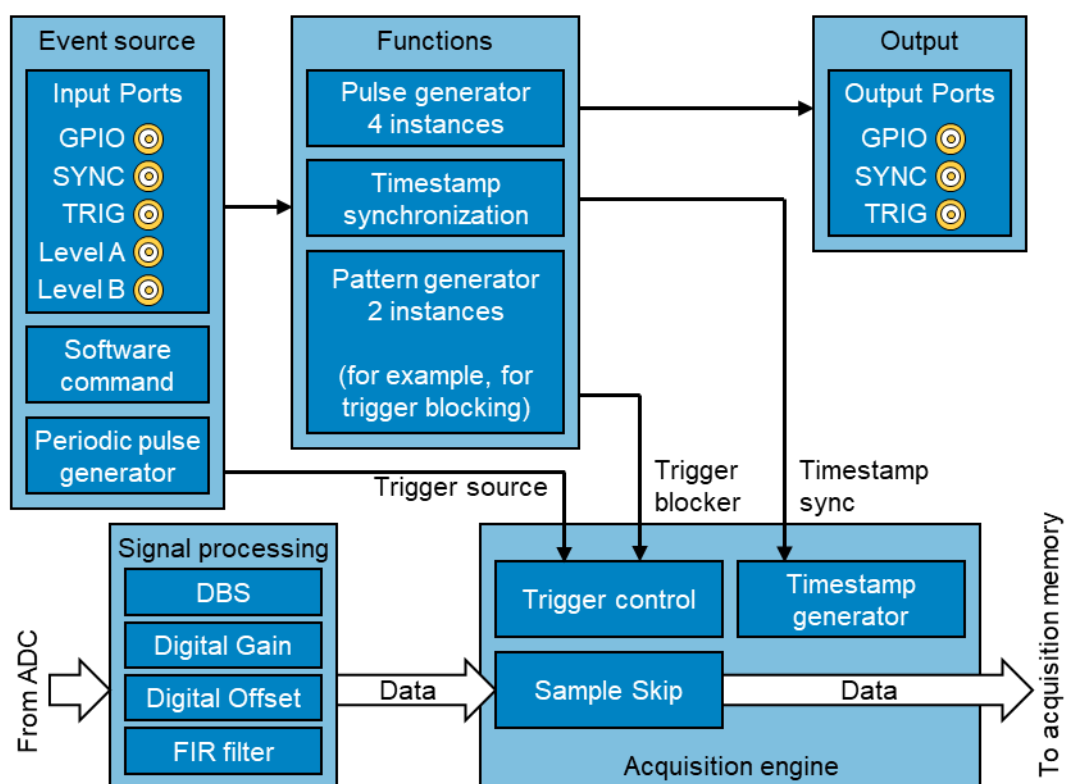


Figure 2 Flow control and synchronization block diagram.

Table 12 Digital signal processing blocks

Object type	Available selections
<b>Digital Signal Processing</b> Included signal processing in the data path for enhanced signal quality.	Digital Baseline Stabilizer (DBS) Digital gain Digital offset Digital FIR filter

**Table 13 Flow control blocks**

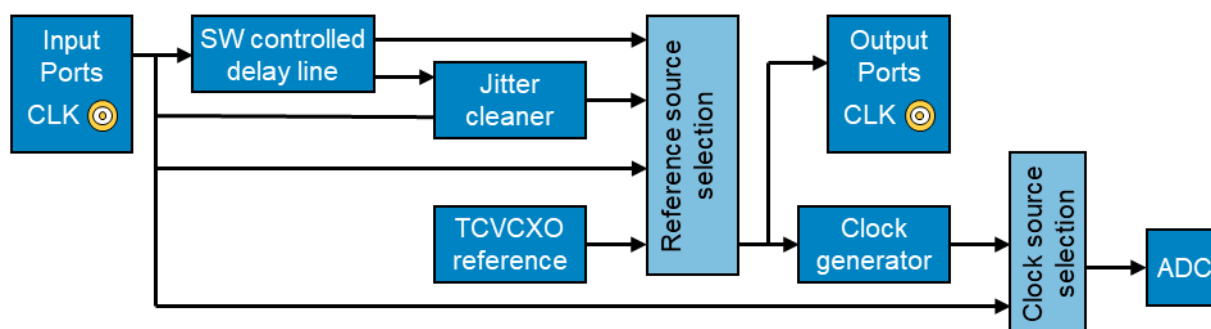
Object type	Available selections
<b>Input ports</b> Electrical connections to the ADQ32 for real-time operation (excluding the PCIe data interface) Used as event source.	Front panel TRIG Front panel SYNC Front panel GPIO Front panel CLK (clock reference or clock input only) Analog channel
<b>Event sources</b> Signals for real-time control of activities in the firmware of ADQ32.	Software command External TRIG External SYNC External GPIO Internal periodic event generator Level analog channel
<b>Functions</b> Included operations for real-time control of activities in the firmware of ADQ32.	Pattern generator for timestamp synchronization Pattern generator general purpose, 2 instances Pulse generator, 4 instances
<b>Output ports</b> Electrical connections to the ADQ32 for real-time operation (excluding the PCIe data interface).	Front panel TRIG Front panel SYNC Front panel GPIO Front panel CLK (clock reference output only)

**Table 14 Firmware functions for flow control**

Function	Modes/selections	Event sources as stimuli
<b>Pattern generator for timestamp synchronization</b> Control the time of the ADQ32-PDRX.		Software command External TRIG External SYNC Internal periodic event generator
<b>Pulse generator</b> Control output pulse shapes. Three instances.	Rising edge Falling edge Pulse length Polarity	Software command External TRIG External SYNC Internal periodic event generator
<b>Pattern generator general purpose</b> For example, used for trigger blocking.	Once Window Gate Trigger counter	Software command External TRIG External SYNC Internal periodic event generator

**Table 15 Firmware functions for acquisition**

Function	Modes	Event Sources as stimuli
<b>Trigger</b> Initiate the acquisition of a data record.		Software command External TRIG External SYNC Internal periodic event generator Level analog channel
<b>Data acquisition modes</b> Configurations for sending digital data to the host PC.	Streaming with header Streaming without header	


**Figure 3 Clock generation block diagram.**
**Table 16 Clock generation**

Function	Modes
<b>Clock reference source</b> Phase and frequency reference for the clock system.	Internal External External with jitter cleaner and/or delay line
<b>Sampling clock sources</b> Actual clock for taking the samples of the analog data.	Internal clock generator Direct external clock
<b>Clock output</b>	Selected clock reference

## **4 FIRMWARE**

### **4.1 FWDAQ**

The FWDAQ is included with all digitizers. The firmware includes control of the hardware and recording of data.

The channel combination is included in FWDAQ for ADQ32-PDRX hardware.

### **4.2 FWATD**

The FWATD is optional. It includes thresholding for noise suppression and accumulations of waveforms. See datasheet 22-2912 for more details.

The channel combination is included in FWATD for ADQ32-PDRX hardware.

### **4.3 Managing firmware**

The digitizer supports multiple firmware images. Note the following about managing firmware images:

- The non-volatile memory on the digitizer can store up to four different firmware images (including the active firmware). Use the tool ADQAssist to change firmware and to upload new images to the digitizer.
- The digitizer (and the enclosing host computer) must be power cycled for the firmware switch to be completed. This is required to let the PCIe bus enumerate with the new firmware.
- Some firmware features require a valid license key to activate. See the ordering information section for details about available firmware features.
- Switching mode between one channel at 5 GSPS and two channels at 2.5 GSPS requires switching the digitizer firmware image.

## 5 ABSOLUTE MAXIMUM RATINGS

**Table 17 Absolute maximum ratings**

Parameter	Condition	Min	Max	Unit
<b>Power supply to GND</b>		-0.4	14	V
<b>Operating temperature</b>		0	45	°C
<b>Analog in to GND Peak</b>		-7	+7	V
<b>Analog in to GND DC</b>		-3	+3	V
<b>TRIG to GND</b>	50-Ω mode	-2	5	V
<b>SYNC to GND</b>	50-Ω mode	-2	5	V
<b>TRIG to GND</b>	500-Ω mode	-2	6	V
<b>SYNC to GND</b>	500-Ω mode	-2	6	V
<b>CLK REF to GND AC amplitude</b>			5	V <sub>pp</sub>
<b>CLK REF to GND DC-level</b>		-5	5	V
<b>GPIO to GND</b>		-1.5	5	V
<b>FFC / FPC differential signal to GND</b>	Powered <sup>23</sup>	-0.5	2.3	V
	Not powered <sup>23</sup>	-0.5	0.5	V
<b>FFC / FPC single-ended signal to GND</b> <sup>23</sup>	Powered <sup>23</sup>	-0.3	3.8	V
	Not powered <sup>23</sup>	-0.3	0.5	V

Exposure to conditions exceeding these ratings may reduce lifetime or permanently damage the digitizer. The digitizer with PCIe format has a built-in fan to cool the device. The built-in temperature monitoring unit will protect the digitizer from overheating by temporarily shutting down parts of the device in an overheat situation.

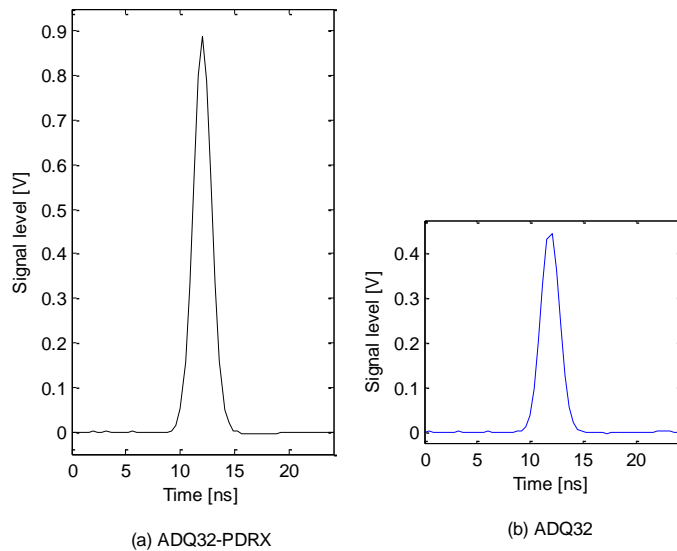
The SMA connectors have an expected lifetime of 500 operations. For frequent connecting and disconnecting of cables, connector savers are recommended.

<sup>23</sup> The absolute maximum ratings depend on whether the ADQ32-PDRX is powered or not. It is recommended to use the respective power rail in the FFC connector to power or enable the external drivers to avoid driving overvoltage into an unpowered digitizer. Use the 1.8 V rail for the differential signals and 3.3 V for the single-ended signals.

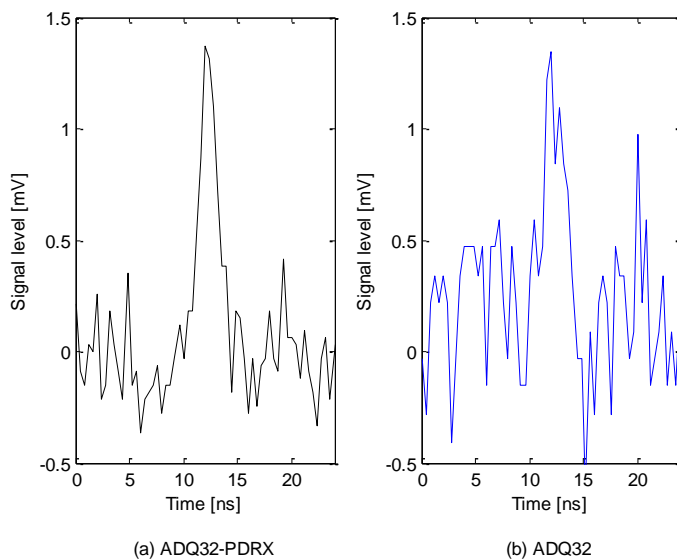
## 6 TYPICAL PERFORMANCE

### 6.1 Time domain pulse data

Pulse examples of different amplitude are plotted showing a ratio greater than 1000 : 1. The pulses are compared with ADQ32 for reference to illustrate the benefit of ADQ32-PDRX in this application. Notice that other applications may benefit from the properties of ADQ32 instead.



**Figure 4 Time domain plot of pulses at 90% of full-scale for the respective digitizer. Notice that ADQ32-PDRX can accept larger signals without overrange**

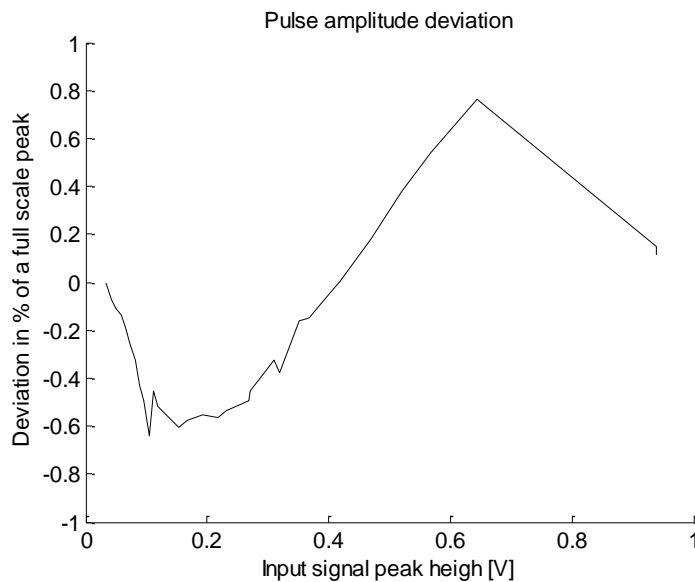


**Figure 5 Time domain plot pulse at 0.6 mV. Notice that the pulse is easier to detect in the ADQ32-PDRX which has lower noise than the ADQ32.**

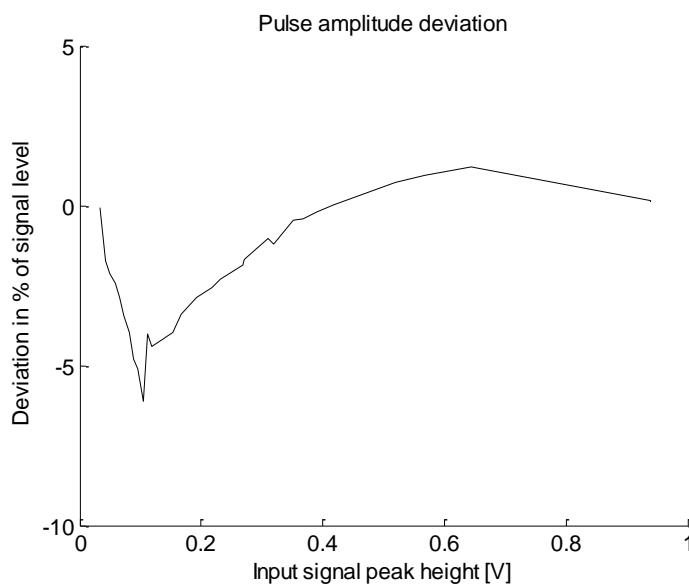
## 6.2 Time domain pulse accuracy

Pulse amplitude accuracy for the combined signal is measured in amplitude sweep.

This is a measurement of the static gain. The amplitude measurement of a wide pulse is related to the input signal amplitude. The deviation from the expected value in percent relative signal level and relative full scale is shown.



**Figure 6 Deviation from ideal pulse height relative to full-scale pulse.**

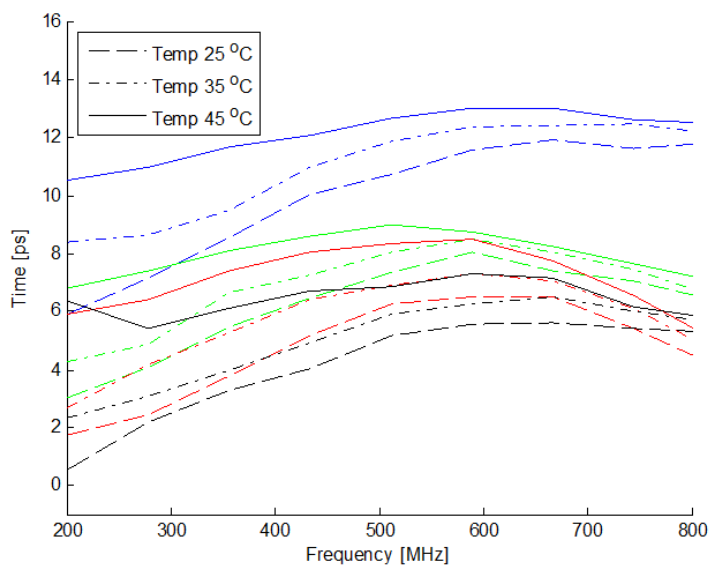


**Figure 7 Deviation from ideal pulse height relative pulse level.**

### 6.3 Timing accuracy

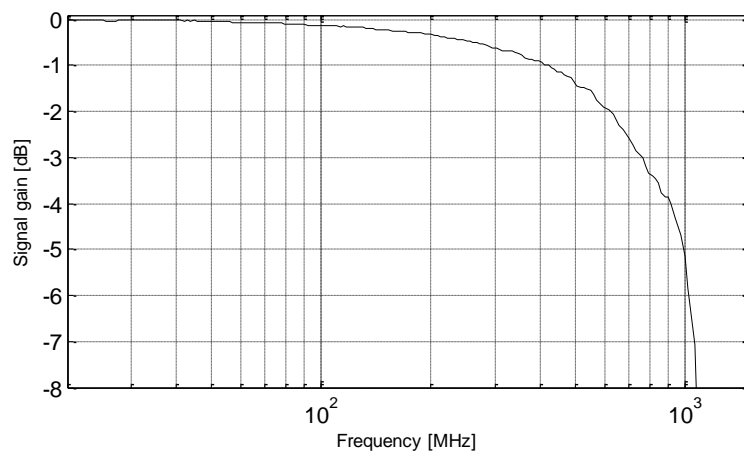
The timing between the branches is measured for frequencies and temperature for 4 units and shown in Figure 8.

A narrow band signal is injected at the input. The phase of the two branches is compared for different frequencies and different ambient temperature. The phase is converted to time difference. This means that pulses in the high gain branch and the low gain branch differ less than 13 ps in time for all 4 boards over temperature.



**Figure 8 Time difference between branches for 4 units over temperature and frequency.**

### 6.4 Frequency response



**Figure 9 Frequency response, typical performance.**

## 7 BLOCK DIAGRAM

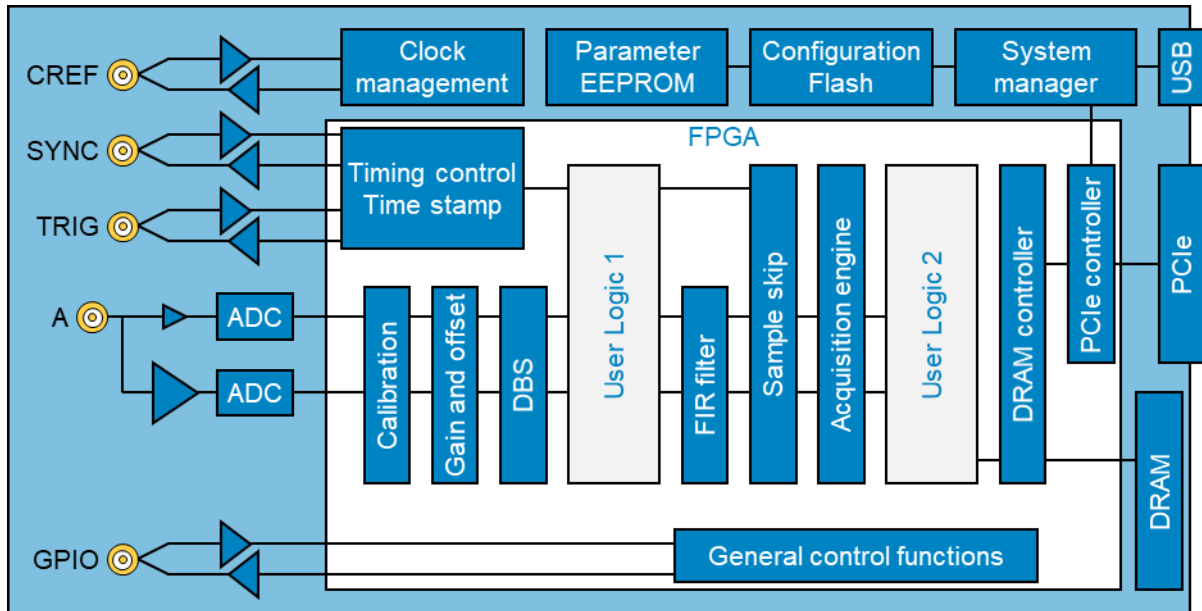


Figure 10 Block diagram ADQ32-PDRX-FWDAQ-PCIe bypass channel combination

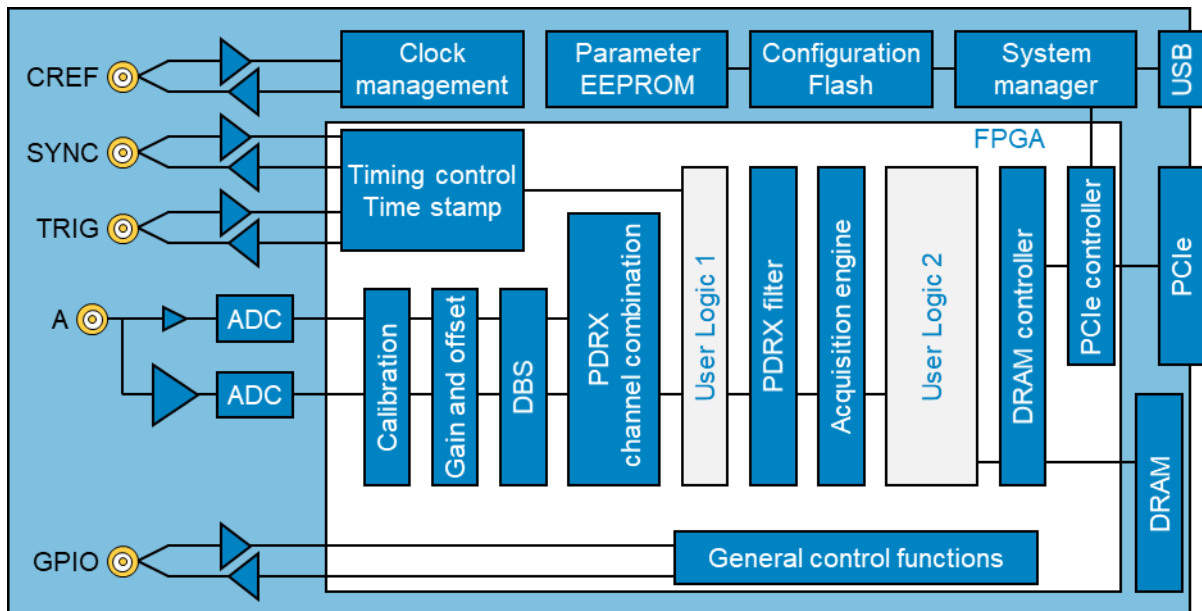


Figure 11 Block diagram ADQ32-PDRX-FWDAC-PCIe

Figure 10 shows a block diagram of ADQ32-PDRX using FWDAQ when the channel combination is bypassed. The two signals with different gain are passed to the user for channel combination.

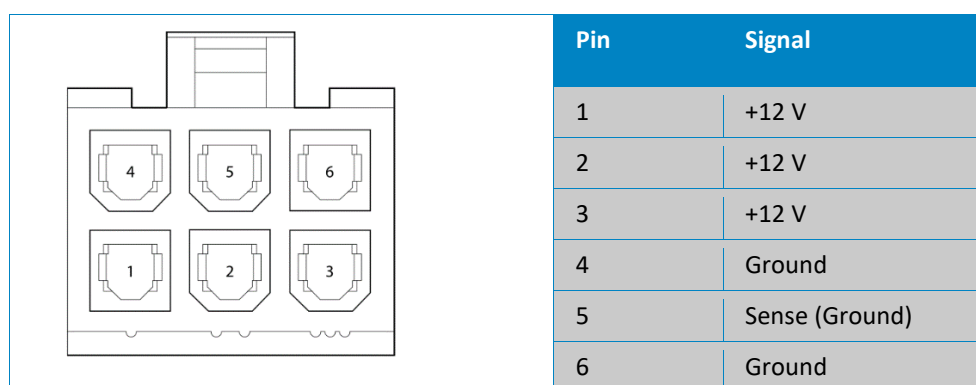
Figure 11 shows a block diagram of ADQ32-PDRX using FWDAC including channel combination. There is only one output channel.

The boxes “User Logic” are open for custom real-signal processing thought the firmware development kit (purchased separately).

## 8 HOST PC INTERFACE PCIE

The ADQ32-PDRX-PCIE is powered from the power supply of the PC via a PCI Express 6-pin (2x3) auxiliary power supply connector. The connection in the cable should be as in Figure 12. A suitable connector is for example Molex 45559-0002.

It is important that the auxiliary power supply is turned on immediately when the PC starts. Otherwise, the digitizer will not be recognized on the PCI Express bus.



**Figure 12 Power supply connection. Cable connector, looking into the connector end.**

## 9 GPIO EXPANSION

The FCP connector allows direct access to the FPGA for building custom expansion boards. The FCP connector requires custom firmware and is accessible through the FPGA development kit. The ADQ32-PDRX user guide document number 21-2539 contains a description of connector.

Note that this connector is connected directly to the FPGA. Damage caused by custom hardware failure is not covered by warranty.

Contact Teledyne SP Devices’ sales representative for more information.

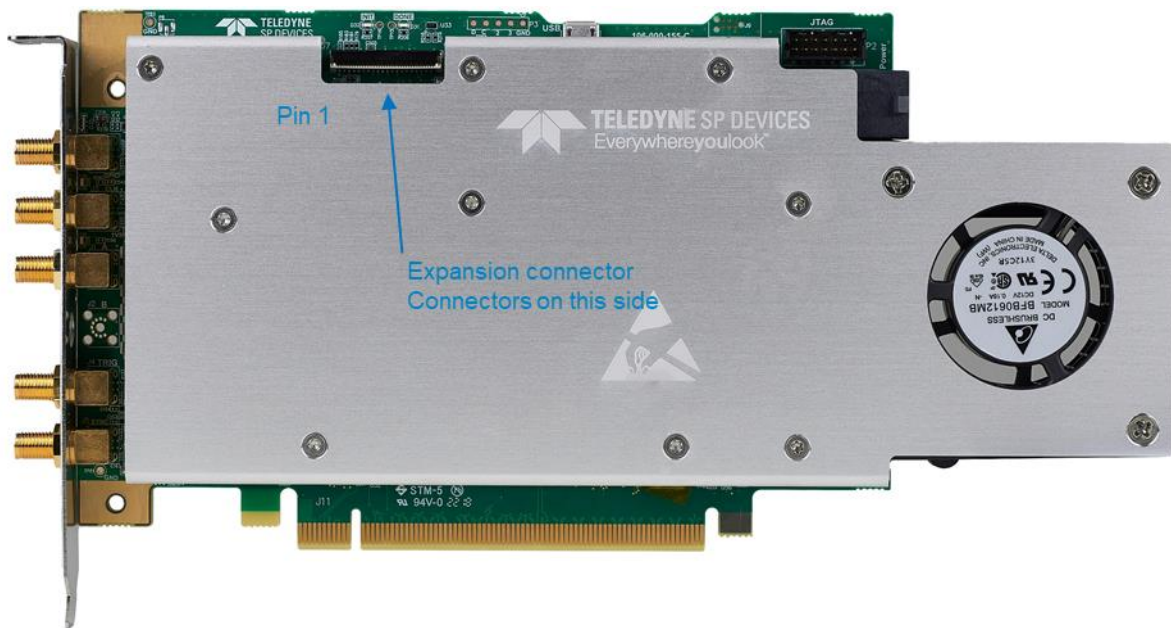


Figure 13 ADQ32-PDRX photo showing GPIO expansion connection on the top side.

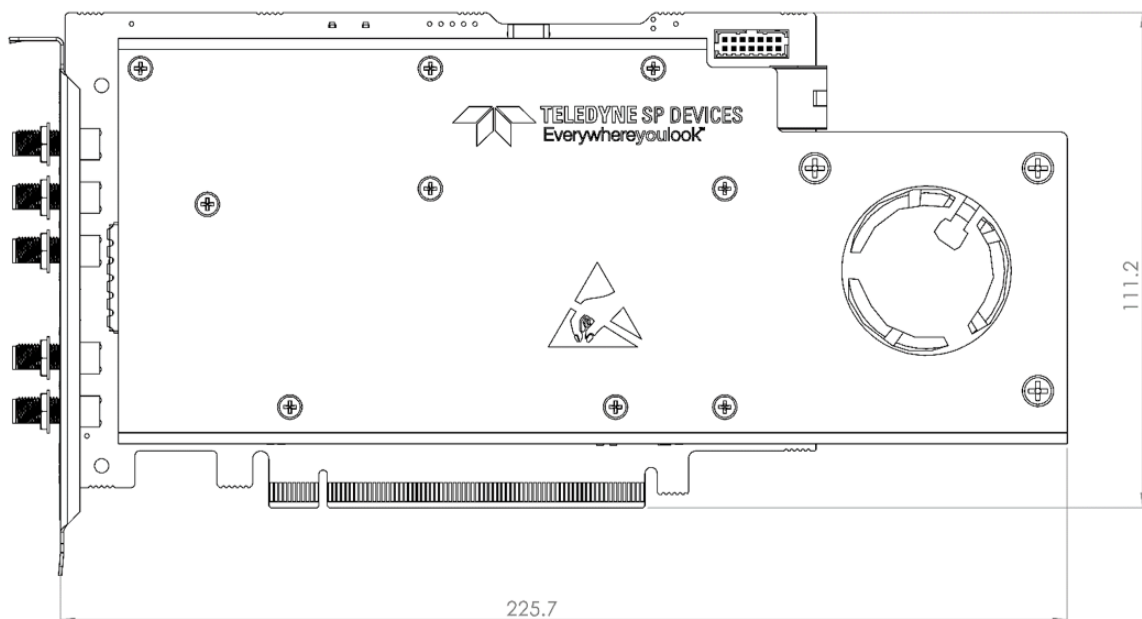


Figure 14 Mechanical drawing

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