

## ADQ33 Datasheet



The ADQ33 is a high-end 12bit dual-channel data acquisition board optimized for use in high-throughput scientific applications. The ADQ33 features

- Two analog input channels
- 1 GSPS per channel
- 7 GByte/s sustained data transfer rate to GPU
- 7 GByte/s sustained data transfer rate to CPU
- Two external triggers
- General Purpose Input/Output (GPIO)
- Open FPGA for real-time signal processing

### Ordering information

- ADQ33 digitizer including firmware FWDAQ, order code **ADQ33**.
- ADQ33 digitizer with warranty extension to 5 years, order code **ADQ33-W5Y**.<sup>1 2</sup>
- Firmware development kit for FWDAQ, order code **ADQ33-DEVDAQ**.

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<sup>1</sup> Included warranty is 3 years from the date the product is shipped by Teledyne SP Devices. The option extends the warranty to 5 years from the date the product is shipped by Teledyne SP Devices.

<sup>2</sup> Warranty extension must be ordered before included 3 years warranty is expired.

## 1 ADQ33 INTRODUCTION

### 1.1 Features

- Two analog input channels
- 1 GSPS sampling rate per channel
- 12 bits vertical resolution
- DC-coupled with 1 GHz bandwidth
- Programmable DC-offset
- Internal and external clock reference
- Internal and external clock source
- Clock reference output
- Internal and external triggers
- 8 GBytes data memory
- 7 GByte/s sustained data streaming to CPU and GPU
- 7 GByte/s peer-to-peer data streaming to GPU
- Data interface PCIe Gen3 x8

### 1.2 Applications

- Swept-Source Optical Coherence Tomography (SS-OCT)
- Time-of-flight Mass Spectrometry
- Distributed Optical Fiber Sensing

### 1.3 Advantages

- A compact high-performance digitizer that optimize the system solution
- Real-time processing and high data throughput
- Teledyne SP Devices' design services are available for fast integration to reduce time-to-market

### 1.4 System design optimization; open FPGA and streaming to CPU and GPU

High-performance data acquisition systems require high speed real-time analysis. ADQ33 offers a variety of options for efficient system design:

#### Streaming to GPU

ADQ33 supports up to 7 GByte/s peer-to-peer streaming and streaming via pinned buffer to GPU. A GPU offers a powerful platform for implementing application-specific signal processing algorithms.

#### Streaming to CPU

ADQ33 supports up to 7 GByte/s to host PC. Implementing the application-specific algorithms in the CPU results in an efficient system.

#### Open FPGA for real-time processing

ADQ33 offers an open FPGA for implementation of the application-specific computations in the FPGA. This gives the most compact system design. Firmware development kit is ordered separately.

## 2 TECHNICAL DATA

Technical parameters are valid for ADQ33 operating with firmware FWDAQ. All parameters are typical unless otherwise noted.

**Table 1 Analog input (front panel label A and B)**

Parameter	Condition	Unit	Min	Typical	Max
<b>Basic parameters</b>					
Number of channels				2	
Sampling rate per channel				1	
Bandwidth	-3dB	GHz		1	
Input range		V <sub>pp</sub>		0.5	
Input impedance		Ω		50	
Coupling				DC	
Connector type				SMA	
<b>Programmable DC-offset</b>					
DC-offset range		V	-0.25		+0.25
<b>Dynamic performance</b>					
Cross talk	< 500 MHz	dBFS		-70	
Noise power density	0 to 500 MHz	dBFS/VHz		-148	
SNR	72 MHz, -1dBFS	dBc		56	
SFDR	72 MHz, -1dBFS	dBc		66	
ENOB relative full scale	72 MHz, -1dBFS	bits		9	

**Table 2 Clock generator and front panel CLK connector**

Parameter	Condition	Unit	Min	Typical	Max
<b>Internal clock reference</b>					
Frequency		MHz		10	
Accuracy		ppm		±3 ±1/year	
<b>Internal sampling clock generator</b>					
Frequency		MHz		1000	
<b>External clock reference input (from front panel CLK connector)<sup>3</sup></b>					
Frequency		MHz	1	10	500
Frequency	Jitter cleaner enabled	MHz	10 -10 ppm	10	10 +10 ppm
Frequency	Delay line used	MHz		10	100
Delay line tuning range		ps		500	
Signal level		Vpp	0.5		3.3
Input impedance	AC	Ω		50	
Input impedance	DC	Ω		10k	
Input impedance (high) <sup>4</sup>	AC	Ω		200	
<b>Clock reference output (on front panel CLK connector)<sup>5</sup></b>					
Frequency		MHz		10	
Signal level	Into 50-Ω load	Vpp		1.2	
Output impedance	AC	Ω		50	
Output impedance	DC	Ω		10k	
<b>External direct sampling clock input (from front panel CLK connector)<sup>6</sup></b>					
Frequency		MHz		1000	
Signal level		Vpp	0.5		3.3
Impedance AC		Ω		50	
Impedance DC		Ω		10k	
<b>Physical connector label CLK</b>					
Connector type				SMA	

<sup>3</sup> Using a clock reference from an external source to synchronize the ADQ33 to the external source.

<sup>4</sup> Software-selectable high-impedance mode.

<sup>5</sup> The internal clock reference of the ADQ33 is made available to synchronize external equipment.

<sup>6</sup> Using an external clock while bypassing the internal clock generator.

**Table 3 Front panel TRIG connector**

Parameter	Condition	Unit	Min	Typical	Max
Connector type				SMA	
<b>Use as input (trigger or GPIO)</b>					
Impedance	DC	$\Omega$		50	
Impedance (high) <sup>7</sup>	DC	$\Omega$		500	
Signal level	50- $\Omega$ mode	V	-0.5		3.3
Adjustable threshold	50- $\Omega$ mode	V	0		2.8
Signal level	High impedance	V	-0.5		5.5
Adjustable threshold	High impedance	V	0		2.3
Pulse repetition frequency	As trigger	MHz			10
Time resolution	As trigger	ps		50	
Update rate	As GPIO	MHz			62.5
<b>Use as output (trigger or GPIO)</b>					
Impedance	DC	$\Omega$		50	
Output level high VOH	Into 50- $\Omega$ load	V	1.8		
Output level low VOL	Into 50- $\Omega$ load	V			0.1
Pulse repetition frequency		MHz			62.5

**Table 4 Front panel SYNC connector (sync is a trigger signal with limited timing resolution)**

Parameter	Condition	Unit	Min	Typical	Max
Connector type				SMA	
<b>Use as input (sync in or GPIO)</b>					
Impedance	DC	$\Omega$		50	
Impedance (high) <sup>7</sup>	DC	$\Omega$		500	
Signal range	50- $\Omega$ mode	V	-0.5		3.3
Adjustable threshold	50- $\Omega$ mode	V	0		2.8
Signal level	High impedance	V	-0.5		5.5
Adjustable threshold	High impedance	V	0		2.3
Pulse repetition frequency	As trigger	MHz			10
Time resolution	As trigger	ns		3.2	
Update rate	As GPIO	MHz			62.5
<b>Use as output</b>					
Impedance	DC	$\Omega$		50	
Output level high VOH	Into 50- $\Omega$ load	V	1.8		
Output level low VOL	Into 50- $\Omega$ load	V			0.1
Pulse repetition frequency		MHz			62.5

<sup>7</sup> Software-selectable high-impedance mode.

**Table 5 Front panel GPIO connector**

Parameter	Condition	Unit	Min	Typical	Max
Connector type				SMA	
<b>Use as input</b>					
Input Impedance		Ω		50	
Impedance (high) <sup>7</sup>		kΩ		10	
Input level high VIH		V	2		
Input level low VIL		V			0.8
Update rate		MHz			62.5
<b>Use as output</b>					
Output Impedance		Ω		50	
Output level high VOH	Into 50-Ω load	V	1.5		
Output level high VOH	No load	V	3.2		
Output level low VOL	Into 50-Ω load	V			0.1
Output level low VOL	No load	V			0.1
Update rate		MHz			62.5

**Table 6 Environment and mechanical parameters**

Parameter	Condition	Unit	Min	Typical	Max
<b>Power and temperature</b>					
Power consumption <sup>8 9</sup>	FWDAQ	W		30	
Power supply		V		12	
Operating temperature	At fan inlet	°C	0		45
<b>Size</b>					
Width				1 slot	
Length		mm		225.7	
Height		mm		111.2	
<b>Compliances</b>					
RoHS3				Yes	
CE				Yes	

<sup>8</sup> Power consumption depend on firmware option.

<sup>9</sup> Power consumption is measured during acquisition and streaming of data at 5 GByte/s to PC.

**Table 7 Data acquisition**

Parameter	Condition	Unit	Min	Typical	Max
Re-arm time		ns			20
Acquisition memory (Data FIFO)	Shared by all channels	GBytes		8	
Record length		samples	16		2 <sup>31</sup>
Pre-trigger <sup>10</sup>		samples	0		16 360
Length granularity, pre-trigger		samples	8		
Trigger delay <sup>11</sup>		samples	0		2 <sup>32</sup> -8
Length granularity, trigger delay		samples	8		

**Table 8 Data transfer**

Parameter	Unit	Value
Supported versions of data transfer standard PCIe		Gen1 Gen2 Gen3
Supported number of lanes		1 4 8
Data rate to CPU sustained with headers	GByte/s	5
Data rate to CPU sustained without headers	GByte/s	7
Data rate to GPU sustained without headers	GByte/s	7
Data rate peer-to-peer to GPU sustained without headers	GByte/s	7

**Table 9 Software support**

Parameter	Value
Operating system	Windows 10 Linux
GUI	Digitizer Studio
Example code	C, Python
API	C / C++

<sup>10</sup> Pre-trigger is set by assigning the parameter “horizontal offset” a negative value

<sup>11</sup> Trigger delay is set by assigning the parameter “horizontal offset” a positive value

### 3 FEATURES FOR DATA FLOW CONTROL, SYNCHRONIZATION AND PROCESSING

The ADQ33 features an advanced machine for flow control, synchronization and signal processing. The block diagrams are shown in Figure 1 and Figure 2. The features are described in the following tables.

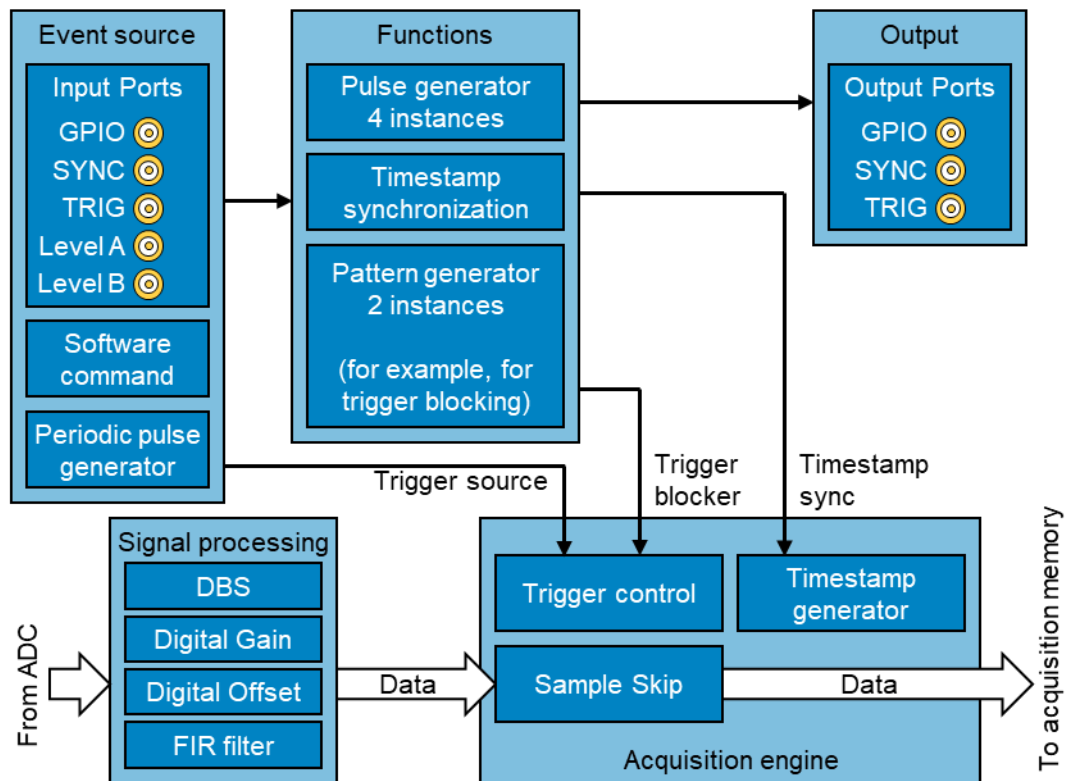


Figure 1 Flow control and synchronization block diagram.

Table 10 Digital signal processing blocks

Object type	Available selections
<b>Digital Signal Processing</b> Included signal processing in the data path for enhanced signal quality.	Digital Baseline Stabilizer (DBS) Digital gain Digital offset Digital FIR filter



**Table 11 Flow control blocks**

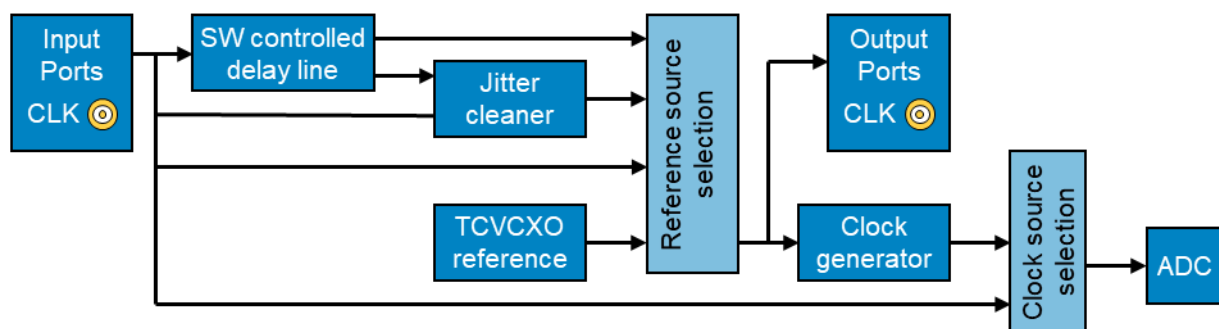
Object type	Available selections
<b>Input ports</b> Electrical connections to the ADQ33 for real-time operation (excluding the PCIe data interface) Used as event source.	Front panel TRIG Front panel SYNC Front panel GPIO Front panel CLK (clock reference or clock input only) Analog channel A Analog channel B
<b>Event sources</b> Signals for real-time control of activities in the firmware of ADQ33.	Software command External TRIG External SYNC External GPIO Internal periodic event generator Level analog channel A Level analog channel B
<b>Functions</b> Included operations for real-time control of activities in the firmware of ADQ33.	Pattern generator for timestamp synchronization Pattern generator for trigger blocking Software-controlled high / low, 3 instances Pulse shaper, 3 instances
<b>Output ports</b> Electrical connections to the ADQ33 for real-time operation (excluding the PCIe data interface).	Front panel TRIG Front panel SYNC Front panel GPIO Front panel CLK (clock reference output only)

**Table 12 Firmware functions for flow control**

Function	Modes / Selections	Event Sources as stimuli
<b>Pattern generator for timestamp sync</b> Control the time of the ADQ33.		Software command External TRIG External SYNC Internal periodic event generator
<b>Pulse generator</b> Control output pulse shapes. Three instances.	Rising edge Falling edge Pulse length Polarity	Software command External TRIG External SYNC Internal periodic event generator
<b>Pattern generator general purpose</b> For example, used for trigger blocking.	Once Window Gate Trigger counter	Software command External TRIG External SYNC Internal periodic event generator

**Table 13 Firmware functions for acquisition**

Function	Modes	Event Sources as stimuli
<b>Trigger</b> Initiate the acquisition of a data record.		Software command External TRIG External SYNC Internal periodic event generator Level analog channel A Level analog channel B
<b>Data acquisition modes</b> Configurations for sending digital data to the host PC.	Streaming with header Streaming without header	


**Figure 2 Clock generation block diagram.**
**Table 14 Clock generation**

Function	Modes
<b>Clock reference source</b> Phase and frequency reference for the clock system.	Internal External External with jitter cleaner and/or delay line
<b>Sampling clock sources</b> Actual clock for taking the samples of the analog data.	Internal clock generator Direct external clock
<b>Clock output</b>	Selected clock reference

#### 4 ABSOLUTE MAXIMUM RATINGS

Table 15 Absolute maximum ratings

Parameter	Condition	Unit	Min	Max
Power supply to GND		V	-0.4	14
Temperature operation		°C	0	45
Analog in to GND		V	-1.75	+1.75
TRIG to GND	50-Ω mode	V	-2	5
SYNC to GND	50-Ω mode	V	-2	5
TRIG to GND	500-Ω mode	V	-2	6
SYNC to GND	500-Ω mode	V	-2	6
CLK REF to GND AC amplitude		V <sub>pp</sub>		5
CLK REF to GND DC-level		V	-5	5
GPIO to GND		V	-1.5	5

Exposure to conditions exceeding these ratings may reduce lifetime or permanently damage the device. The digitizer with PCIe format has a built-in fan to cool the device. The built-in temperature monitoring unit will protect the digitizer from overheating by temporarily shutting down parts of the device in an overheat situation.

The SMA connectors have an expected lifetime of 500 operations. For frequent connecting and disconnecting of cables, connector savers are recommended.

## 5 TYPICAL PERFORMANCE

### 5.1 Frequency response

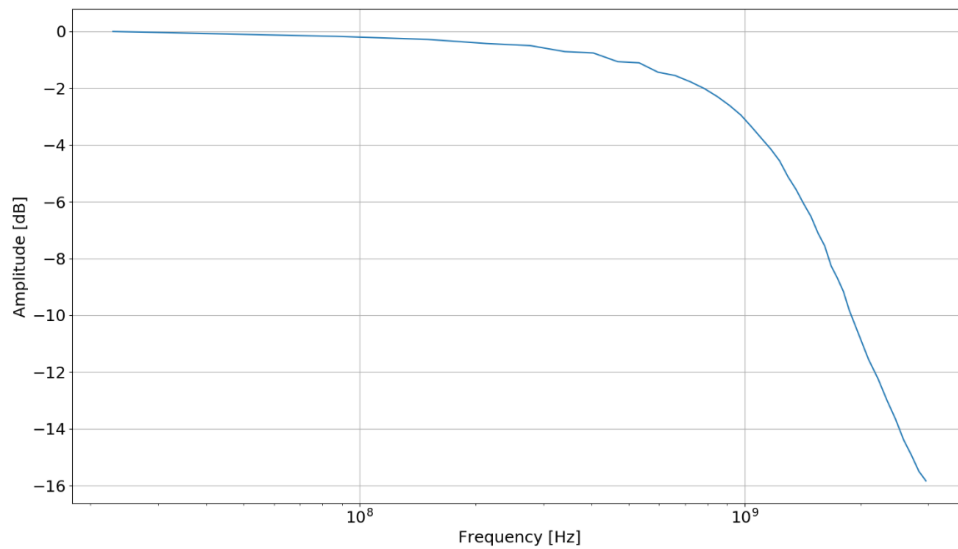


Figure 3 Frequency response, typical performance.

### 5.2 FFT

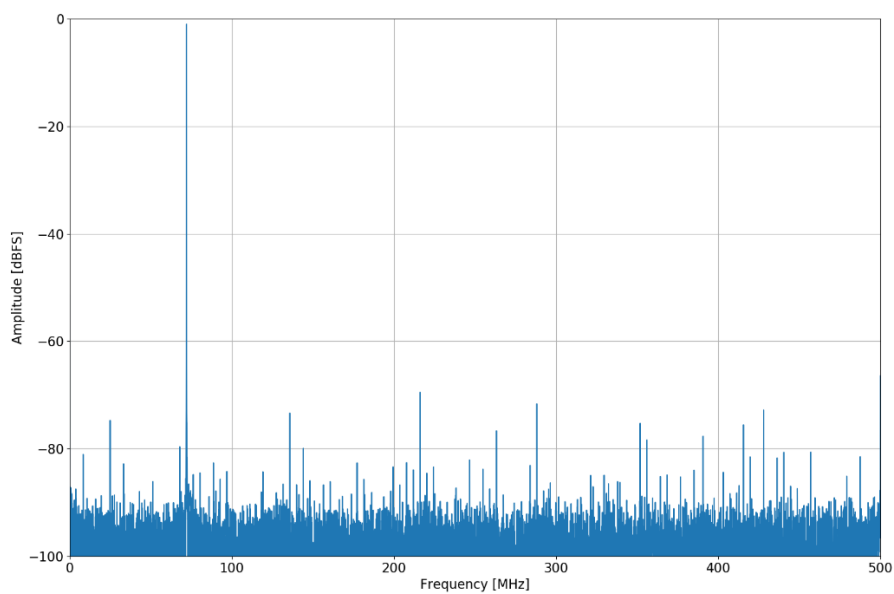
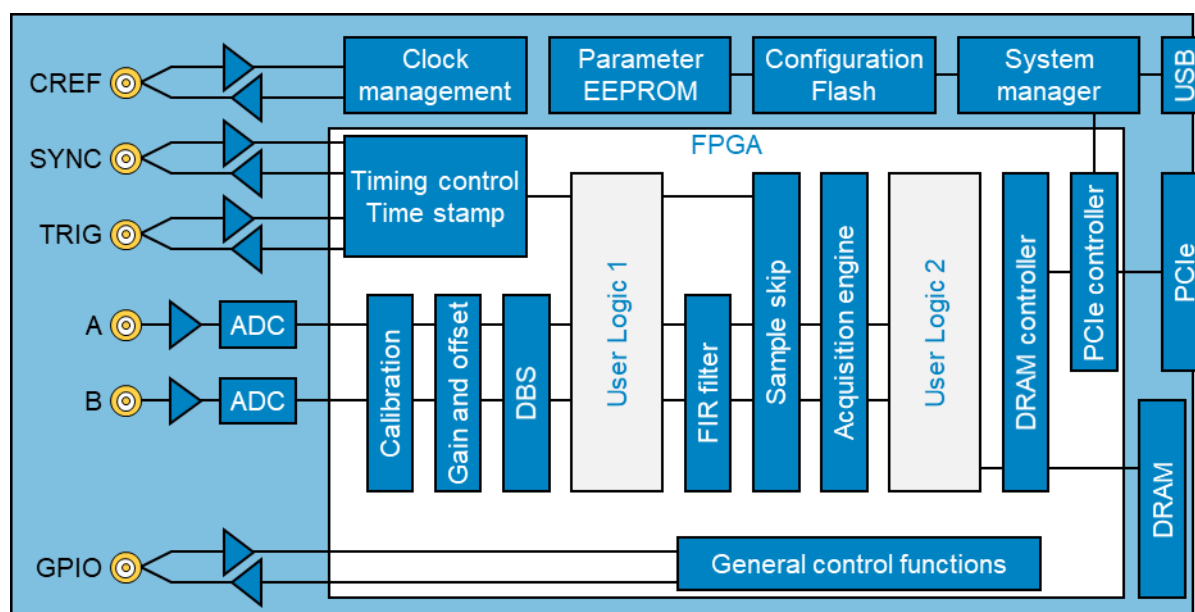


Figure 4 FFT typical single-tone performance.

## 6 BLOCK DIAGRAM



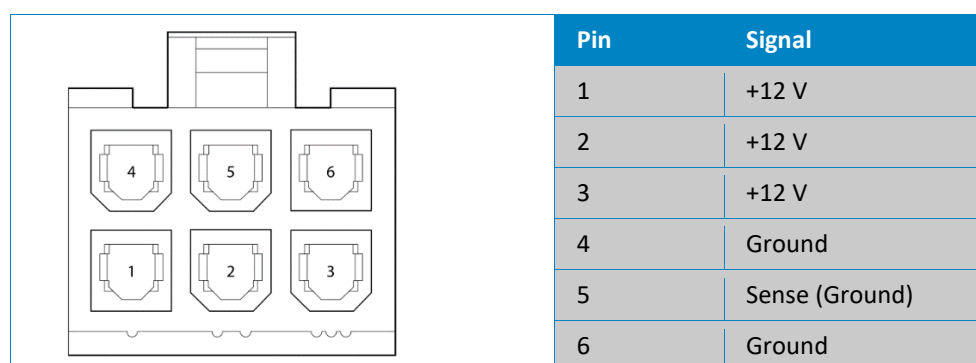
**Figure 5 Block diagram**

Figure 5 shows a block diagram of ADQ33. The boxes “User Logic” are open for custom real-signal processing through the firmware development kit (purchased separately).

## 7 HOST PC INTERFACE PCIE

The ADQ33-PCIE is powered from the power supply of the PC via a PCI Express 6-pin (2x3) auxiliary power supply connector. The connection in the cable should be as in Figure 6. A suitable connector is for example Molex 45559-0002.

It is important that the auxiliary power supply is turned on immediately when the PC starts. Otherwise, the digitizer will not be recognized on the PCI Express bus.



**Figure 6 Power supply connection. Cable connector, looking into the connector end.**

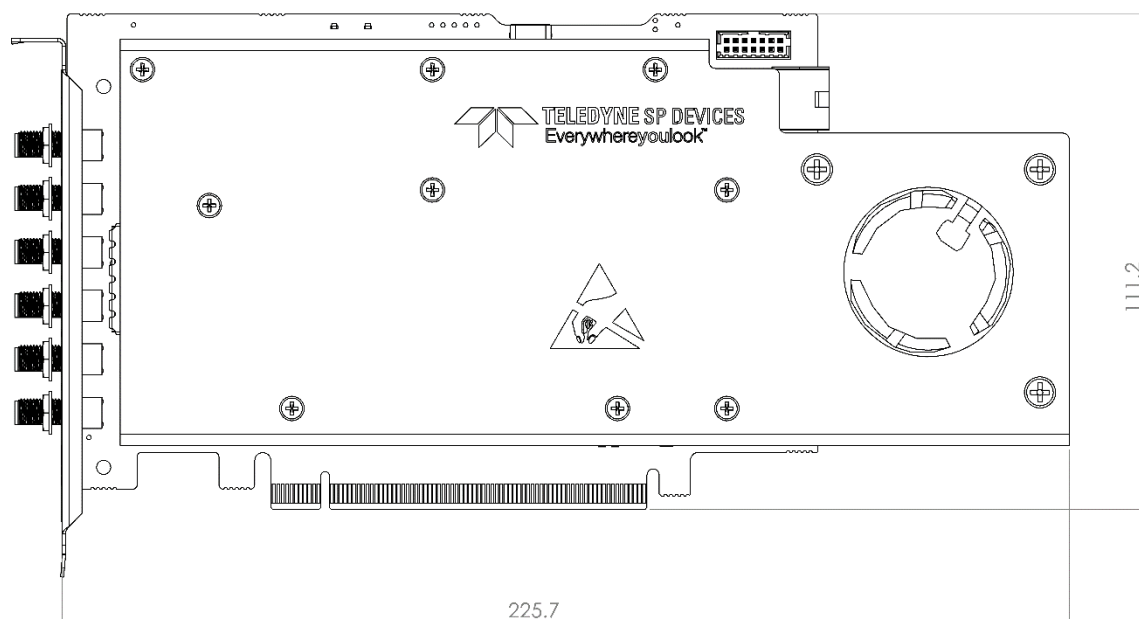


Figure 7 Mechanical drawing



Figure 8 ADQ33 photo

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## Teledyne SP Devices Corporate Headquarters

Teknikringen 6  
SE-583 30 Linköping  
Sweden

Phone: +46 (0)13 465 0600

Fax: +46 (0)13 991 3044

Email: [info@spdevices.com](mailto:info@spdevices.com)

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