M2p.75xx-x4 - 32 channel digital I/O card

- **32 digital I/O channels**
- **1 kS/s up to 125 MS/s sampling speed**
- **Ultra Fast PCI Express x4 interface**
- **110 Ohm input impedance selectable**
- **Inputs 3.3 V and 5.0 V TTL compatible**
- **1 GByte of on-board memory**
- **700 MB/s FIFO mode for input and output**
- **Synchronization of up to 16 cards per system**
- **Features: Single-Shot, Streaming, Multiple Recording/Replay, Gated Sampling/Replay, Sequence Mode, Timestamps**
- **Direct data transfer to CUDA GPU using SCAPP option**

SCAPP
Spectrum's CUDA Access – Parallel Processing

M2p series

- PCIe x4 Gen 1 Interface
- Works with x4/x8/x16* PCIe slots
- Sustained streaming mode up to 700 MB/s**
- Half-length PCIe Form Factor

Operating Systems	Recommended Software	Drivers
• Windows 7 (SP1), 8, 10, Server 2008 R2 and newer • Linux Kernel 2.6, 3.x, 4.x, 5.x • Windows/Linux 32 and 64 bit	• Visual C++, Delphi, GNU C++, VB.NET, C#, Java, Python, Julia • SBench 6	• MATLAB • LabVIEW

	Input		Output	
Model	16 bit	32 bit	16 bit	32 bit
M2p.7515-x4	125 MS/s	125 MS/s	125 MS/s	125 MS/s

General Information

The M2p.75xx series of fast digital I/O cards allow to acquire or replay digital patterns with a programmable speed of up to 125 MS/s. The direction can be switched by software between input (digital data acquisition) and output (digital pattern generation). The on-board memory of 1 GByte can be completely used for digital pattern. Furthermore the on-board memory can be switched to a FIFO buffer allowing to continuously stream data in either output or input direction.

Using the unique M2p-Star-Hub up to 16 different cards of the M2p series can be synchronized in one system. The M2p series offers - besides the M2p.75x digital I/O card - 16 bit digitizers with 5 MS/s to 125 MS/s sampling speed and up to 8 channels and 16 bit AWGs with 40 MS/s to 125 MS/s sampling speed and up to 8 channels.

*Some x16 PCIe slots are for the use of graphic cards only and can't be used for other cards.**Throughput measured with a motherboard chipset supporting a TLP size of 256 bytes.

Software Support

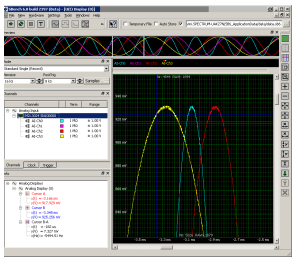
Windows drivers

The cards are delivered with drivers for Windows 7, Windows 8 and Windows 10 (each 32 bit and 64 bit). Programming examples for Visual C++, C++ Builder, Delphi, Visual Basic, VB.NET, C#, Python, Java and Julia are included.

Linux Drivers

All cards are delivered with full Linux support. Pre compiled kernel modules are included for the most common distributions like Fedora, Suse, Ubuntu LTS or Debian. The Linux support includes SMP systems, 32 bit and 64 bit systems, versatile programming examples for GNU C++, Python and Julia, as well as the possibility to get the kernel driver sources for your own compilation.

SBench 6

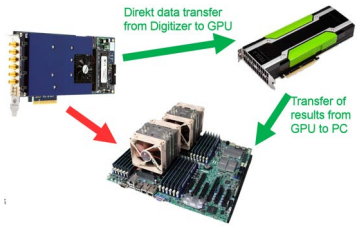


A base license of SBench 6, the easy-to-use graphical operating software for Spectrum cards, is included in the delivery. The base license makes it is possible to test the card, display acquired data and make some basic measurements. It's a valuable tool for checking the card's performance and assisting with the unit's initial setup. The cards also come with a demo license for the SBench 6 professional version. This license gives the user the opportunity to test the additional features of the professional version with their hardware. The professional version contains several advanced measurement functions, such as FFTs and X/Y display, import and export utilities as well as support for all acquisition modes including data streaming. Data streaming allows the cards to continuously acquire data and transfer it directly to the PC RAM or hard disk. SBench 6 has been optimized to handle data files of several GBytes. SBench 6 runs under Windows as well as Linux (KDE, GNOME and Unity) operating systems. A test version of SBench 6 can be downloaded directly over the internet and can run the professional version in a simulation mode without any hardware installed. Existing customers can also request a demo license for the professional version from Spectrum. More details on SBench 6 can be found in the SBench 6 data sheet.

Third-party products

Spectrum supports the most popular third-party software products such as LabVIEW or MATLAB. All drivers come with detailed documentation and working examples are included in the delivery.

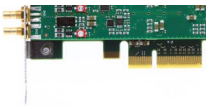
SCAPP – CUDA GPU based data processing



For applications requiring high performance signal and data processing Spectrum offers SCAPP (Spectrum's CUDA Access for Parallel Processing). The SCAPP SDK allows a direct link between Spectrum digitizers, AWGs or Digital Data Acquisition Cards and CUDA based GPU cards. Once in the GPU users can harness the processing power of the GPU's multiple (up to 10000) processing cores and large (up to 48 GB) memories. SCAPP uses an RDMA (Linux only) process to send data at the full PCIe transfer speed to and from the GPU card. The SDK includes a set of examples for interaction between the Spectrum card and the GPU card and another set of CUDA parallel processing examples with easy building blocks for basic functions like filtering, averaging, data demultiplexing, data conversion or FFT. All the software is based on C/C++ and can easily be implemented, expanded and modified with normal programming skills.

General Hardware features and options

PCI Express x4

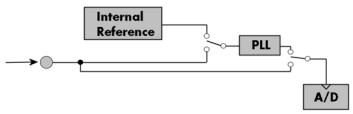


The M2p series cards use a PCI Express x4 Gen 1 connection. They can be used in PCI Express x4, x8 and x16 slots with hosts supporting Gen 1, Gen 2, Gen 3 or Gen4. The maximum sustained data transfer rate is more than 700 MByte/s (read direction) or 700 MByte/s (write direction) per slot. Physically supported slots that are electrically connected with only x1 or x2 can also be used with the M2p series cards, but with reduced data transfer rates.

External clock I/O

Using a dedicated line a sampling clock can be fed in from an external system. It's also possible to output the internally used sampling clock to synchronize external equipment to this clock.

Reference clock



The option to use a precise external reference clock (typically 10 MHz) is necessary to synchronize the instrument for high-quality measurements with external equipment (like a signal source). It's also possible to enhance the stability of the sampling clock in this way. The driver automatically generates the requested sampling clock from the fed in reference clock.

Star-Hub

The Star-Hub is an additional module allowing the phase stable synchronization of up to 16 boards in one system. Two versions are available: one with up to 6 cards and the large version supports up to 16 cards in one system. Both versions can be mounted in two different ways, to either extend the cards length to ¾ PCIe length occupying one slot, or extend its width to two slots whilst keeping the ½ PCIe length.

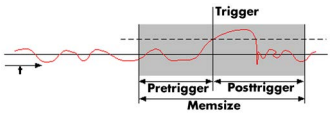
Independent of the number of boards there is no phase delay between the channels. The Star-Hub distributes trigger and clock information between all boards. As a result all connected boards are running with the same clock and the same trigger. All trigger sources can be combined with OR/AND. For digitizers that means all channels of all cards to be trigger source at the same time.

Multi-Purpose I/O

As standard each card has 4 multi-purpose I/O lines. All I/O lines can be used for asynchronous digital I/O, can carry additional status information or can be used as trigger inputs.

Input (Digital Data Acquisition) features

Ring buffer mode

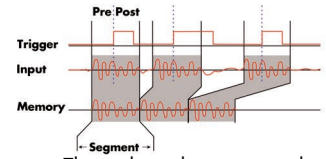


The ring buffer mode is the standard mode of all oscilloscope instruments. Digitized data is continuously written into a ring memory until a trigger event is detected. After the trigger, post-trigger samples are recorded and pre-trigger samples can also be stored. The number of pre-trigger samples available simply equals the total ring memory size minus the number of post trigger samples.

FIFO mode

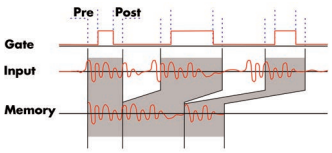
The FIFO or streaming mode is designed for continuous data transfer between the card and the PC memory. When mounted in a PCI Express x4 Gen 1 interface both, read and write streaming speeds of up to 700 MByte/s are possible. The control of the data stream is done automatically by the driver on interrupt request basis. The complete installed on-board memory is used to buffer the data, making the continuous streaming process extremely reliable.

Multiple Recording



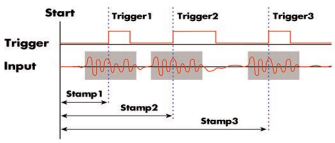
The Multiple Recording mode allows the recording of several trigger events with an extremely short re-arming time. The hardware doesn't need to be restarted in between. The on-board memory is divided in several segments of the same size. Each of them is filled with data if a trigger event occurs. Pre- and posttrigger of the segments can be programmed. The number of acquired segments is only limited by the used memory and is unlimited when using FIFO mode.

Gated Sampling



The Gated Sampling mode allows data recording controlled by an external gate signal. Data is only recorded if the gate signal has a programmed level. In addition a pre-area before start of the gate signal as well as a post area after end of the gate signal can be acquired. The number of gate segments is only limited by the used memory and is unlimited when using FIFO mode.

Timestamp



The timestamp function writes the time positions of the trigger events in an extra memory. The timestamps are relative to the start of recording, a defined zero time, externally synchronized to a radio clock, an IRIG-B a GPS receiver. Using the external synchronization gives a precise time relation for acquisitions of systems on different locations.

Output (Pattern Generation) features

Singleshot output

When singleshot output is activated the data of the on-board memory is played exactly one time. The trigger source can be either one of the external trigger inputs or the software trigger. After the first trigger additional trigger events will be ignored.

Repeated output

When the repeated output mode is used the data of the on-board memory is played continuously for a programmed number of times or until a stop command is executed. The trigger source can be either one of the external trigger inputs or the software trigger. After the first trigger additional trigger events will be ignored.

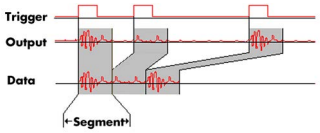
Single Restart replay

When this mode is activated the data of the on-board memory will be replayed once after each trigger event. The trigger source can be either the external TTL trigger or software trigger.

FIFO mode

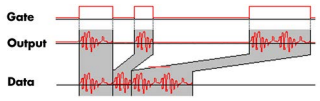
The FIFO or streaming mode is designed for continuous data transfer between the card and the PC memory. When mounted in a PCI Express x4 Gen 1 interface both, read and write streaming speeds of up to 700 MByte/s are possible. The control of the data stream is done automatically by the driver on interrupt request basis. The complete installed on-board memory is used to buffer the data, making the continuous streaming process extremely reliable.

Multiple Replay



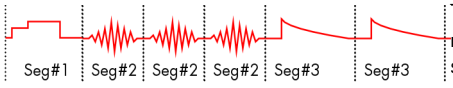
The Multiple Replay mode allows the fast output generation on several trigger events without restarting the hardware. With this option very fast repetition rates can be achieved. The on-board memory is divided into several segments of the same size. Each segment can contain different data which will then be played with the occurrence of each trigger event.

Gated Replay



The Gated Sampling mode allows data replay controlled by an external gate signal. Data is only replayed if the gate signal has attained a programmed level.

Sequence Mode



The sequence mode allows to split the card memory into several data segments of different length. These data segments are chained up in a user chosen order using an additional sequence memory. In this sequence memory the number of loops for each segment can be programmed and trigger conditions can be defined to proceed from segment to segment. Using the sequence mode it is also possible to switch between replay waveforms by a simple software command or to redefine waveform data for segments simultaneously while other segments are being replayed. All trigger-related and software-command-related functions are only working on single cards, not on star-hub-synchrnonized cards.

Technical Data

Only figures that are given with a maximum reading or with a tolerance reading are guaranteed specifications. All other figures are typical characteristics that are given for information purposes only. Figures are valid for products stored for at least 2 hours inside the specified operating temperature range, after a 30 minute warm-up, after running an on-board calibration and with proper cooled products. All figures have been measured in lab environment with an environmental temperature between 20°C and 25°C and an altitude of less than 100 m.

Power Up

Data channels direction after power up		input (high impedance)
Clock and trigger output after power up		disabled

Digital Data Inputs

Direction	software programmable	all channels input or all channels output (no mixed direction)	
Acquisition channel selection	software programmable	16 or 32	
Sampling clock edge	software programmable	rising or falling edge (see clock section for details)	
Logic type		3.3V LVTTL (5V TTL tolerant) with bus-hold as floating input protection	
Input transition rise or fall rate		≤ 10 ns/V	
Input Impedance	software programmable	110 Ω / 50 kΩ || 15 pF	
110 Ω termination voltage		2.25 V	
Standard input levels		Low: ≤ 0.8 V	High: ≥ 2.0 V
Absolute maximum Input levels		Low: ≥ –0.5 V	High: ≤ 7.0 V
Input current sink	no termination	Low: -5.0µA (0.0 V)	High:+5.0µA (3.3V), +20.0µA (5.0V)

Digital Data Outputs

Direction	software programmable	all channels input or all channels output (no mixed direction)	
Replay channel selection	software programmable	16 or 32	
Update clock edge	software programmable	rising or falling edge (see clock section for details)	
Logic type		3.3V LVTTL	
Typical output levels	high impedance	Low: 0.2 V	High: 2.8 V
Output max current load		Low: 64 mA	High: -32 mA
Output levels at max load		Low: < 0.5 V	High: > 2.0 V
Output Impedance (typical)		ca. 7 Ω	
Stop level	software programmable	Tristate, Low, High, Hold Last, Custom Value	

Output Data Delays

Trigger to 1st sample	78 samples
Gate end to last replayed sample	78 samples

Trigger

Available trigger modes	software programmable	External, Software, Or/And, Delay	
Trigger edge	software programmable	Rising edge, falling edge or both edges	
Trigger pulse width	software programmable	0 to [4G - 1] samples in steps of 1 sample	
Trigger delay	software programmable	0 to [4G - 1] samples in steps of 1 samples	
Trigger holdoff (for Multi, ABA, Gate)	software programmable	0 to [4G - 1] samples in steps of 1 samples	
Multi, ABA, Gate: re-arming time		< 40 samples (+ programmed pretrigger + programmed holdoff)	
Pretrigger at Multi, ABA, Gate, FIFO	software programmable	8 up to [32 kSamples / number of active channels] in steps of 8	
Posttrigger	software programmable	8 up to [8G - 4] samples in steps of 8 (defining pretrigger in standard scope mode)	
Memory depth	software programmable	16 up to [installed memory / number of active channels] samples in steps of 8	
Multiple Recording/ABA segment size	software programmable	8 up to [installed memory / number of active channels] samples in steps of 8	
Internal/External trigger accuracy		1 sample (sampled with programmed clock edge, see clock section for details)	
Timestamp modes	software programmable	Standard, Startreset, external reference clock on X1 (e.g. PPS from GPS, IRIG-B)	
Data format		Std., Startreset:	64 bit counter, increments with sample clock (reset manually or on start)
		RefClock:	24 bit upper counter (increment with RefClock) 40 bit lower counter (increments with sample clock, reset with RefClock)
Extra data	software programmable	none, acquisition of X0/X1/X2/X3 inputs at trigger time, trigger source (for OR trigger)	
Size per stamp		128 bit = 16 bytes	
External trigger sources		**X0, X1, X2, X3**	
External trigger logic type		3.3V LVTTL (5V TTL tolerant)	
Input transition rise or fall rate		≤ 10 ns/V	
External trigger impedance	software programmable	110 Ω / 50 kΩ || 15 pF	
110 Ω termination voltage		2.25 V	
Standard input levels		Low: ≤ 0.8 V	High: ≥ 2.0 V
Absolute maximum Input levels		Low: ≥ –0.5 V	High: ≤ 7.0 V
Input current sink	no termination	Low: -5.0µA (0.0 V)	High:+5.0µA (3.3V), +20.0µA (5.0V)
External trigger bandwidth		125 MHz	
Minimum external trigger pulse width		≥ 2 samples	

Multi Purpose I/O lines

Number of multi purpose input/output lines		four, named X0, X1, X2, X3	
Multi Purpose line		**X0, X1, X2, X3**	
Input: available signal types	software programmable	Asynchronous Digital-In, Timestamp Reference Clock, Logic trigger	
Input: logic type		3.3V LVTTL (5V TTL tolerant)	
Input transition rise or fall rate		≤ 10 ns/V	
Input: impedance	software programmable	110 Ω / 50 kΩ || 15 pF	
Input: 110 Ω termination voltage		2.25 V	
Input: standard levels		Low: ≤ 0.8 V	High: ≥ 2.0 V
Input: absolute maximum levels		Low: ≥ –0.5 V	High: ≤ 7.0 V
Input current sink	no termination	Low: -5.0µA (0.0 V)	High:+5.0µA (3.3V), +20.0µA (5.0V)
Input: maximum bandwidth		125 MHz	
Output: available signal types	software programmable	Run-, Arm-, Trigger-Output, Asynchronous Digital-Out	
Output: logic type		3.3V LVTTL	
Output: typical levels	high impedance	Low: 0.2 V	High: 2.8 V
Output: max current load		Low: 64 mA	High: -32 mA
Output: levels at max load		Low: < 0.5 V	High: > 2.0 V
Output: impedance (typical)		ca. 7 Ω	
Output: update rate (synchronous modes)		sampling clock (on programmed clock edge, see clock section for details)	

Clock

Clock Modes	software programmable	internal PLL, external clock, external reference clock, sync
Active clock edge	software programmable	rising or falling edge
Internal clock range (PLL mode)	software programmable	1 kS/s to 125 MS/s
Internal clock accuracy	after warm-up	≤ ±1.0 ppm (at time of calibration in production)
Internal clock aging		≤ ±0.5 ppm / year
PLL clock setup granularity (int. or ext. reference)		1 Hz
External reference clock range	software programmable	128 kHz up to 125 MHz
Direct external clock to internal clock delay		5.0 ns
Direct external clock range		DC to 125 MHz
Direct external clock minimum LOW/HIGH time		4 ns
Clock input: logic type		3.3V LVTTL (5V TTL tolerant)
Clock input: transition rise or fall rate		≤ 10 ns/V
Clock input: impedance	software programmable	110 Ω / 50 kΩ || 15 pF
Clock input: 110 Ω termination voltage		2.25 V
Clock input: standard levels		Low: ≤ 0.8 V, High: ≥ 2.0 V
Clock input: absolute maximum levels		Low: ≥ –0.5 V, High: ≤ 7.0 V
Clock input: current sink (no termination)	no termination	Low: -5.0µA (0.0 V), High:+5.0µA (3.3V), +20.0µA (5.0V)
External reference clock input duty cycle		45% - 55%
Clock output: logic type		3.3V LVTTL
Clock output: typical levels	high impedance	Low: 0.2 V, High: 2.8 V
Clock output: max current load		Low: 64 mA, High: -32 mA
Clock output: levels at max load		Low: < 0.5 V, High: > 2.0 V
Clock output: impedance (typical)		ca. 7 Ω
Synchronization clock multiplier „N" for different clocks on synchronized cards	software programmable	N being a multiplier (1, 2, 3, 4, 5, ... Max) of the card with the currently slowest sampling clock. The card maximum sampling rate must not be exceeded.

Connectors

Digital Inputs/Outputs	40 pole half pitch (Hirose FX2 series) Connector on card: Hirose FX2B-40PA-1.27DSL Flat ribbon cable connector: Hirose FX2B-40SA-1.27R	Cable-Type: Cab-d40-xx-xx

Connection Cycles

All connectors have an expected lifetime as specified below. Please avoid to exceed the specified connection cycles or use connector savers.

Hirose FX2 connector	500 connection cycles
PCIe connector	50 connection cycles

Environmental and Physical Details

Dimension (Single Card) type M2p.65x3, M2p.65x8, M2p.654x or M2p.657x	8 channel AWG or High power AWG	L x H x W: 168 mm (½ PCIe length) x 107 mm x 30 mm. Requires one additional slot right of the main card's bracket, on „component side" of the PCIe card.
Dimension (all other single cards)		L x H x W: 168 mm (½ PCIe length) x 107 mm x 20 mm (single slot width)
Dimension (with -SH6tm or -SH16tm installed)		Extends W by 1 slot right of the main card's bracket, on „component side" of the PCIe card.
Dimension (with -SH6ex or -SH16ex installed)		Extends L to 245 mm (¾ PCIe length) at the back of the PCIe card
Dimension (with -DigSMB or -DigFX2 installed)		Extends W by 1 slot left of the main card's bracket, on „solder side" of the PCIe card.
Weight (M2p.59xx, M2p.75xx series)	maximum	215 g
Weight (M2p.65x0, M2p.65x1, M2p.65x6 series)	maximum	195 g
Weight (M2p.65x3, 65x8, 654x, 657x series)	maximum	305 g
Weight (Star-Hub Option -SH6ex, -SH6tm)	including 6 sync cables	65 g
Weight (Star-Hub Option -SH16ex, -SH16tm)	including 16 sync cables	90 g
Weight (Option -DigSMB)		50 g
Weight (Option -DigFX2)		60 g
Warm up time		10 minutes
Operating temperature		0 °C to 40 °C
Storage temperature		-10 °C to 70 °C
Humidity		10% to 90%
Dimension of packing	1 or 2 cards	470 mm x 250 mm x 130 cm
Volume weight of packing	1 or 2 cards	4 kgs

PCI Express specific details

PCIe slot type	x4, Generation 1
PCIe slot compatibility (physical)	x4, x8, x16
PCIe slot compatibility (electrical)	x1, x2, x4, x8, x16 with Generation 1, Generation 2, Generation 3, Generation 4
Sustained streaming mode (Card-to-System: M2p.59xx or M2p.75xx)	> 700 MB/s (measured with a chipset supporting a TLP size of 256 bytes, using PCIe x4 Gen1)
Sustained streaming mode (System-to-Card: M2p.65xx or M2p.75xx)	> 700 MB/s (measured with a chipset supporting a TLP size of 256 bytes, using PCIe x4 Gen1)

Certification, Compliance, Warranty

According to EN ISO/IEC 17050-1:2010

EMC Compliance	Compliant with CE Mark Electromagnetic Compatibility Directive 2014/30/EU (EMC) Applied Standards: EN 55032: 2016 (CISPR 32) EN 61000-4-2: 2009 (IEC 61000-4-2) EN 61000-4-3: 2011 (IEC 61000-4-3)
Safety Compliance	Compliant with CE Mark Low Voltage Directive 2014/35/EU (LVD) Applied Standards: IEC 61010-1: 2010 / EN 61010-1: 2010
RoHS Compliance	RoHS Directive 2015/863/EC RoHS Directive 2011/65/EC (RoHS II) RoHS Directive 2002/95/EC (RoHS)
REACH Compliance	REACH directive 2006/1907/EC
Product warranty	5 years starting with the day of delivery
Software and firmware updates	Life-time, free of charge

Power Consumption

	3.3V	12V	Total
M2p.75xx	TBD A	TBD A	TBD W

MTBF

MTBF	TBD hours

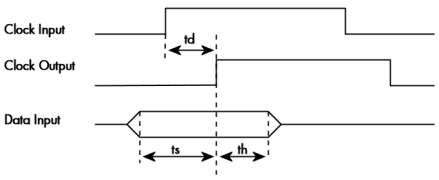
Clock to data timing

The setup and hold times as well as any delays relate to the output clock. Please be sure to meet this timing constraints if feeding in external clock. All timings shown here are in relation to the programmed clock edge (rising or falling). The illustration on the right shows the relation to the rising edge as an example.

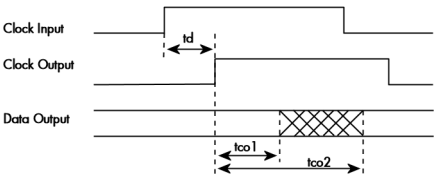
For detailed information on the different modes for external clocking please refer to the dedicated chapter in the hardware manual for the boards of the M2p.75xx series.

Input	Parameter	External Clocking (direct and reference clock)	Internal Clocking
Clock Input to Clock Output (single card)	t_d	9.3 ns	n.a.
Clock In to Clock Out (Star-Hub connected)	t_d	TBD	n.a.
Data/Trigger Output	t_{co1}	0.0 ns	0.0 ns
	t_{co2}	2.0 ns	2.0 ns
Data/Trigger Input	t_s	6.1 ns	6.1 ns
	t_h	-3.5 ns	-3.5 ns

Input timing

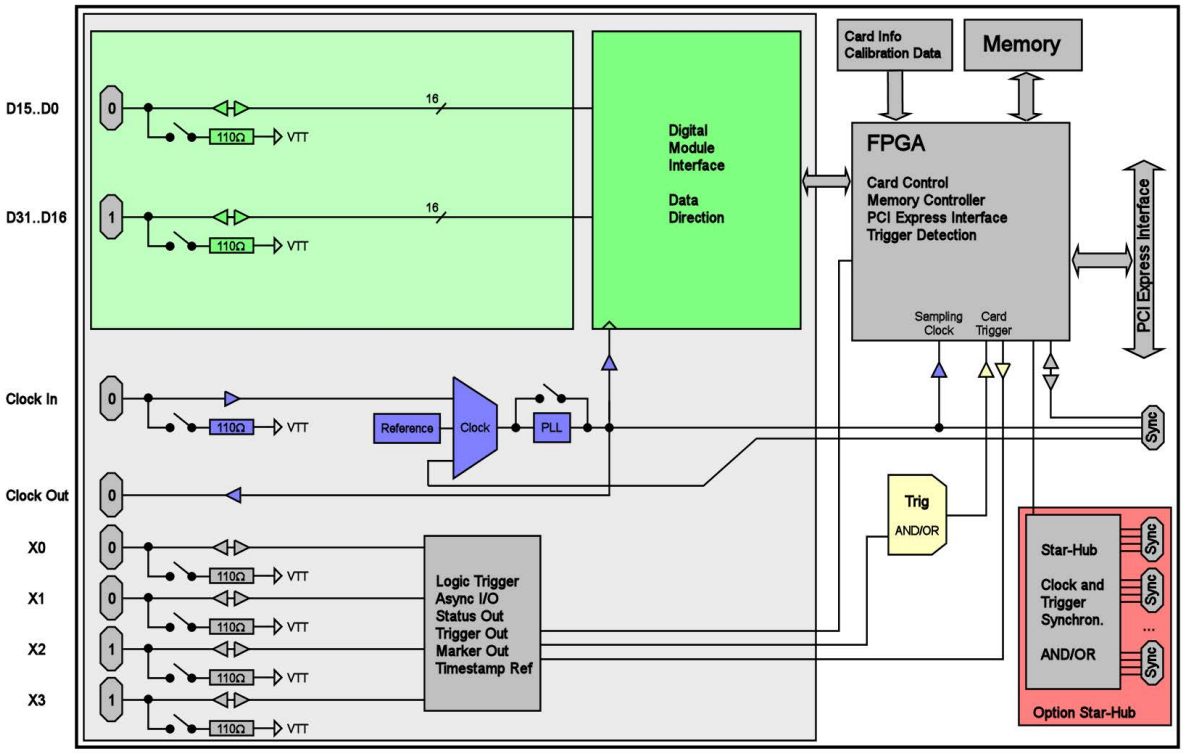


Output timing



When using external clock, a delayed clock signal is generated on the Clock Output pin. The timing data in relation to this delayed clock output is identical to the timing when using internal clocking. It is therefore strongly recommended that you use the delay clock output for clocking any external devices.

Hardware block diagram



Order Information

The card is delivered with 1 GByte on-board memory and supports standard acquisition and replay (scope, single-shot, loop, single restart), FIFO acquisition/replay (streaming), Multiple Recording/Replay, Gated Sampling/Replay, Timestamps and Sequence Mode. Operating system drivers for Windows/Linux 32 bit and 64 bit, examples for C/C++, LabVIEW (Windows), MATLAB (Windows and Linux), .NET, Delphi, Java, Python, Julia and a Base license of the oscilloscope software SBench 6 are included.

One digital connecting cable Cab-d40-idc-100 is included in the delivery for every digital connection (each 16 channels).

PCI Express x4

Order no.	Input	Output	Speed
M2p.7515-x4	32 Channels	32 Channels	125 MS/s

Options

Order no.	Option
M2p.xxxx-SH6ex [1]	Synchronization Star-Hub for up to 6 cards incl. cables, only one slot width, card length 245 mm
M2p.xxxx-SH6tm [1]	Synchronization Star-Hub for up to 6 cards incl. cables, two slots width, standard card length
M2p.xxxx-SH16ex [1]	Synchronization Star-Hub for up to 16 cards incl. cables, only one slot width, card length 245 mm
M2p.xxxx-SH16tm [1]	Synchronization Star-Hub for up to 16 cards incl. cables, two slots width, standard card length
M2p-upgrade	Upgrade for M2p.xxxx: Later installation of options Star-Hub

Cables

	Option
Cab-d40-idc-100	Flat-ribbon cable to 2x20 pole IDC, 100 cm
Cab-d40-d40-100	Flat-ribbon cable to 40 pole FX2, 100 cm

Software SBench6

Order no.	
SBench6	Base version included in delivery. Supports standard mode for one card.
SBench6-Pro	Professional version for one card: FIFO mode, export/import, calculation functions
SBench6-Multi	Option multiple cards: Needs SBench6-Pro. Handles multiple synchronized cards in one system.
Volume Licenses	Please ask Spectrum for details.

Software Options

Order no.	
SPc-RServer	Remote Server Software Package - LAN remote access for M2i/M3i/M4i/M4x/M2p/M5i cards
SPc-SCAPP	Spectrum's CUDA Access for Parallel Processing - SDK for direct data transfer between Spectrum card and CUDA GPU. Includes RDMA activation and examples.

[1] : Just one of the options can be installed on a card at a time.

[2] : Third party product with warranty differing from our export conditions. No volume rebate possible.

Technical changes and printing errors possible